


ANSI/VITA 6-1994

Approved as an American National Standard by 

American National Standard
for Signal Computing System Architecture (SCSA)

Secretariat

VMEbus International Trade Association

Approved July 24, 1995

American National Standards Institute, Inc.



VMEbus INTERNATIONAL TRADE ASSOCIATION

7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260 USA

PH: 480-951-8866, FAX: 480-951-0720

E-mail: info@vita.com, URL: <http://www.vita.com>

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Abstract

The Signal Computing System Architecture (SCSA) specification establishes a framework for the inter- and intra-system transfer of serial media data and control information oriented toward the development of high density call and voice processing products and systems. The SCSA architecture is application specific and is embodied as a family of buses that are defined in this physical layer of the specification to reside on the VMEbus J2/P2 connector. The SCSA buses coexist with products compliant with ANSI/VITA 1-1994, VME64.

SCSA at the physical level consists of two separate subbuses, a sixteen line, TDM data transfer bus called the SCbus, and a serial, peer-to-peer communication link called the SCmessage bus. The primary purpose of the SCbus is to support the exchange of real time telephonic voice, facsimile, data, video and other media streams. The purpose of the SCmessage bus is to transport interprocess control and status messages. This specification defines only the physical and data link OSI layers of the eventual four layer transport facility.

The SC data transport bus is a synchronous, byte-serial, continuously framed bus organized as 16 serial data paths each divided into 32, 64, or 128 eight bit timeslots with a frame rate of 8,000 per second in order to accommodate intra-system telephonic voice and data transfers. The message bus is an HDLC framed, 2 Mbps, CSMA/CD packet bus that is bit-synchronized with the data transport bus.

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Published by

**VMEbus International Trade Association
7825 E. Gelding Drive., Suite 104, Scottsdale, AZ 85260**

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Printed in the United States of America

ISBN 1-885731-04-3

Foreword (This foreword is not part of the VITA Standard)

This standard was processed and submitted to the VME-SCSA Technical Review Committee of the VFEA International Trade Association(VITA) of Scottsdale, AZ, USA. The committee unanimously approved this standard by formal ballot. At the time of the approval of this standard the VME-SCSA committee had the following members:

Ray Alderman, acting Chairman of the Standards Organization of the VFEA International Trade Association(VITA)

Michael Humphrey, Executive Director, VITA

Louis Francz, Moderator, Dialogic Corp, Parsippany NJ

Organizations Represented:

CSP, Inc.....	Paul Vena
DY 4 Systems, Inc.	Jing Kwok*
Electronic Solutions, Inc.....	Frank Hom
Hybricon, Corp.	Michael Munroe*
Matrix Corp.....	Dick DeBock*
MITRE Corp.	Malcolm Airst
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Motorola Corp.	Chau Pham
Object Technology, Inc.	Kim Clohessy
PEP Modular Computers	Ray Alderman*
Precision Software, Inc.	Rob Brayton*
.....	Wally Williams*
Northern Telecom, Ltd.....	Bruce Wallace
Schroff, Inc.....	Michael Thompson

*contributory only

The SCSA architecture was originally developed and proposed in 1992 by Dialogic Corporation, Parsippany, NJ. to provide an industry standard by which to promote third party developer involvement in the IBM PC compatible(ISA platform) call and voice processing environment.

The current VME market need for high functionality voice processing products provided the ideal environment into which to introduce SCSA. With limited choices in the way of toll quality voice store and forward, telephony interface, voice recognition, speech synthesis or switching capability, the VME 6U merchant board market was not serving the telecom and voice system developers well.

This specification covers the hardware specific elements of the VME-SCSA subbus including the message bus OSI protocol layers 1 and 2. Subsequent specifications will be written to provide an interface definition for the device specific software layer that will provide compatibility between compliant VME-SCSA products and available upper layer SCSA resource management application programming interface(api) and other application software.

SCSA, when fully specified will comprise a set of stable interfaces within which multi-vendor system functional elements can be interconnected and provide a high degree of interoperability to developers and users.

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CHAPTER 1

1. Introduction to Signal Computing System Architecture(SCSA)

1.1. Definitions

1.1.1. ASIC: Application Specific Integrated Circuit. Typically, an ASIC refers to a gate array or standard cell.

1.1.2. Bit Integrity: The ability of a digital transport mechanism to provide a bit for bit replica at it's receiving end the information presented to it's transmitting end.

1.1.3. Board: Any hardware module that controls it's own physical interface to the SCbus. It is also referenced as "module" or card.

1.1.4. Channel: A transmission path on the SCbus data bus or SCmessage bus that transmits data between two points. It is also used in reference to a telephony talk circuit within a digital public switched network trunk.

1.1.5. Clear Channel: In telephony context, an octet organized digital transport mechanism that is code transparent, thus providing bit integrity; as in 64 kb/s clear channel capability.

1.1.6. Clock master: A system module that is currently driving the system clocks and sync pulse to the SCbus.

1.1.7. Clock slave: A system module that can receive and synchronize to the SCbus timing signals and exchange data with the SCbus.

1.1.8. Clock source: A system module that is capable of deriving the required system clocks either from an external source or internal generator.

1.1.9. DTMF: Dual tone multi-frequency. An international system of telephony signaling digit transmission based on a 2 out of 8 audio tone combination. Each combination represents a numeral of zero through 9, star(*), pound(#), or one of four special characters called a, b, c, or d. These are defined in ITU-T recommendation Q.23.

1.1.10. Digital Service: A PSTN 4-wire, switched access arrangement containing time division multiplexed and companded telephonic audio circuits and the associated signaling for those circuits or channels.

1.1.11. Frame, data: Time slots are grouped together into frames for synchronization purposes. The number of time slots in each frame depends on the SCbus clock rate. However each frame has a fixed period of 125 ms. Frames are delineated by the timing signal FSYNC*.

1.1.12. Frame, message: Control and signaling data transmitted on the SCbus or SCmessage bus is encapsulated in a data link layer frame. The form of a SCmessage bus frame is fully compliant with ISO-HDLC UI (Unnumbered Information) Frame specifications.

1.1.13. Functional Module: A collection of electronic circuitry that resides on the VME bus and or SCSA bus and works with other system elements to perform a task.

1.1.14. HDLC: High-level Data Link Control. ISO standard #3309, bit oriented, data link layer protocol used for the transmission of data and messages on the SCbus.

1.1.15. Host CPU: The VME bus CPU that contains the SCSA device software or drivers.

1.1.16. Hyperchannel: A data path on the SCbus made up of more than one time slot. By bundling time slots into a hyperchannel data path, a time-coherent channel bandwidth greater than 64 Kbps can be realized.

1.1.17. ITU-T: The International Telecommunications Union, telephony sub group. The organization assumed responsibility for establishing guidelines for international telecommunications technical standards from the previous CCITT.

1.1.18. Idle: A state of the SCbus or SCmessage bus where no information is being transmitted and the bus line is pulled high.

1.1.19. Message Bus(SCmessage bus): An CSMA/CD based and HDLC framed inter-module communication link implemented on a single wire bus and referenced to the SCbus clock.

1.1.20. Module: In the context of this document, a plug-in VME compliant printed circuit functional system component. It is also called a "board"

1.1.21. Network: In the context of this document, the public switched telephone network providing switched analog or digital access with dial-up station to station addressing and audio, data or video bearer channel services.

1.1.22. Network module: A system component carrying electronics for interfacing a voice or signal processing system to the public telephone network. It fulfills the electrical and regulatory requirements for that connection and provides for the routing of SCbus timeslots to and from the PSTN. It is capable of providing network synchronized timing (clocks) to the system.

1.1.23. Node: An independent SCSA system unit or chassis in a distributed processing SCSA network, consisting of one or more resource and/or network boards.

1.1.24. Octet: Per ITU-T, a digital, binary, eight-bit data item or quantity. In this context, an octet is equivalent to a byte of data.

1.1.25. PLL: Phase Locked Loop. An electronic circuit that locks the frequency of a locally generated clock oscillator to and attenuates the phase jitter from an external reference clock.

1.1.26. PCM: Pulse Code Modulation. In the context of this document, encoded and companded speech or audio signal samples.

1.1.27. PSTN: Public Switched Telephone Network.

1.1.28. Port: In the context of this document, a port is an interface point where an external communication channel is terminated and information is exchanged.

1.1.29. Resource module: A system component carrying electronics for signal processing, for example voice recognition or text-to-speech processing. It provides a function or service to the system. It is also referenced as a server or function server.

1.1.30. SC2000: An ASIC of VLSI Technology, Inc. that provides access to the SCSA TDM signal bus and also buffers signals to the SCmessage passing bus.

1.1.31. SCSA: Signal Computing System Architecture. A generalized, open-standard architecture describing the components and standard interfaces for a generalized, telephony connected signal processing system.

SCSA describes all elements of the system architecture from the electrical characteristics of the SCbus to the high level device programming interfaces or API's.

1.1.32. SCSA compatible product: A generic term applied to hardware and/or software products that comply with the appropriate parts of the SCSA model, functionality and interface definitions.

1.1.33. SCbus: The standard bus for intra-node communication(board-to-board inside a box). The SCbus features a hybrid bus architecture consisting of a serial Message Bus for control and signaling, and a 16 wire, bit-serial TDM data bus.

1.1.34. SCbus ASIC: A custom IC, such as the SC2000, that is specially designed for SC transport bus access.

1.1.35. SCSA product: A product that complies with the defined SCSA standards for data and signaling transfer. Device specific software will complete integration into the VME-SCSA platform.

1.1.36. SD bus: The generic term applied to the 16 isochronous. bit-serial TDM SCbus data signals.

1.1.37. Standby module: A module that is prepared to be SCbus clock master when the current clock module stops providing clocks and FSYNC and releases CLKFAIL.

1.1.38. Stream: For the purpose of this document one of the 16 physical data lines making up the **SCbus** TDM data bus.

1.1.39. System administrator: A term used in this document to represent a system functional component that manages events, and resources in a physical VME system.

1.1.40. TDM: Time Division Multiplexed signal stream.

1.1.41. TLP: Transmission level point. The equivalent digitally encoded analog content reference level which when a 1 milliwatt signal is applied produces from a unity gain decoder an analog signal which equals the TLP value in dBm: i.e.: at a TLP -3 point a 1 mw signal is represented by a (neg)3 dBm digitally encoded analog content.

1.1.42. TTS: Text-to-speech. A software technology that converts binary coded text such as ASCII names and numbers to streams of isochronous speech samples, typically PCM coded at an 8 KHz sample rate for transmission to the telephony network.

1.1.43. Time slot: The smallest switchable data unit on the SCbus. A time slot consists of 8 consecutive serial bits of data. One time slot is equivalent to a TDM voice or data circuit with 64 Kbps bandwidth.

1.1.44. VME compliant: Modules that conform to all mandatory aspects of both IEEE 1014, as revised, and VITA-1-1994 VME64 standards.

1.1.45. VR: Voice recognition. The software technology that converts streams of isochronous voice samples of spoken words or numerals to binary coded text or digits.

1.1.46. VOX: An abbreviation for PCM coded voice samples as in a VOX file.

1.1.47. Voice Module: - A functional module that performs the storage, and playback of telephonic audio signals, detects DTMF and other tone signals and performs PSTN signaling.

1.2. Application System Objectives

The systems that are integrated using the functional elements described herein along with other VME system components are used for, but not limited to the capture and dissemination of speech, data, video and other signals commonly found on the public telephone network. The capture and dissemination capability provided by these systems is incorporated by system developers into various services that are either made available or offered for a charge to the public at large or to subscribing groups of users as part of value-added communication facilities. In the main, these SCSA based systems and services mediate between pairs of human callers, between client computers or between humans and computers.

Specifically, these application systems provide the voice and other media access that are offered as services commonly known as voice mail, voice response, predictive or programmed dial-and-deliver, value-added (premium rate) call routing, fax storage and forward as well as fax server capabilities. Often these services are bundled into feature packages and sold generically as call center management packages.

These voice processing systems may be connected directly to the public network or may be attached to customer premise equipment such as a PBX. Alternatively, call processing systems may also be connected between the public network and the customer premise switching equipment or live operators. A substantial amount of this equipment is connected in the telephone operating companies' central offices as a means of providing alternate operator services or information operator assistance, voice mail and value-added call dialing or routing.

1.3. SCSA Objectives

The primary objective for VME-SCSA is to provide internal and external standards that promote the development of high performance call and media processing systems. An important secondary SCSA objective is to provide an architecture that has sufficient capability and expansion room to handle advances in voice, data and image technology for several product generations.

Specifically, this physical level VME-SCSA document provides standards for the internal system distribution of digitally encoded, telephonic audio and other real time signals between functional modules and to facilitate communication between those modules at a low-overhead architectural level.

Secondarily, this specification seeks to encourage the development of out-of-chassis links to other suitably equipped chassis such that SCbus media streams, telephone connections and resource channels may be shared or routed so as to affect a larger logical system.

1.4. Signal Computing System Architectural Model

The VME-SCSA model for voice processing extends the existing VME market model for a functionally decomposed system built around commercially available boards and packaging components. The current large merchant market for functional modules includes CPU, memory, disk storage, peripheral control and communication along with the system packaging that permits practical deployment.

SCSA permits voice and other compliant functional modules of various manufacture to interoperate with each other in the exchange and distribution of voice, fax, video, image and data in an integrated "voice" application system. The SCSA voice system model further permits multiple voice modules to cooperate in providing the needed system channel capacity along with support for specialized modules for voice recognition, text to speech conversion, local telephone interface and PSTN trunk access.

The SCSA software model provides isolation between the application and the physical voice facilities so as to provide signal routing, resource allocation and assignment as well as the simplification of network access protocols.

The SCSA model is designed to allow physically distributed systems to share data and resources. The SCSA software model will include addressing and routing to allow system-to-system control and global allocation of resources and routing of data regardless of location or point of entry or exit to the network.

1.5. Introduction to the VME-SCSA Physical Level Specification

1.5.1. Specification Objectives

This specification is intended to provide all the necessary information to implement a VME-SCSA compatible functional module at the physical level. Normative, interpretive and illustrative references are provided in Appendix A to give readers insight into the purpose behind certain requirements where the intent is not self-evident.

Subsequent specifications will be developed to add the module software element interface to SCSA. These software interface specifications will provide access for third party developed subsystems to standardized upper layer SCSA resource management(API) software.

1.5.2. Interface Element Description

The VME-SCSA architecture is a compatible adjunct to the VMEbus specification primarily to serve the popular 6U by 160 mm. board market. This does not preclude it's use on 9U format boards (as per IEEE 1101.1) but the VMEbus standard IEEE 1014-1987 does not define this board type.

This architecture contains both a mechanical and a functional structure. The mechanical packaging is expected to comply with and is embodied in the VME Bus specifications chapter 7(ref. #2 and #3) and in IEEE P1101.10. In this specification there are added definitions of previously defined USER I/O pins on the J2/P2 pinout(see Table 10).

The functional portions of this standard electrically and logically describe: (a)the SCSA subbuses, (b)how each subbus works. This standard defines transactions between functional modules; the rules which govern bus operations are detailed in text and diagrams.

1.5.3. Signal definitions

The following is the detailed description of each transport bus signal:

SCLK System clock - driven by the clock master. The clock frequency is selectable. It can be either 2.048M, 4.096M, or 8.192M Hz. SCLK is used to identify the data bit positions on the SCbus. The positive going edge indicates the beginning of the bit. The bus clock tolerance should be within the specification of stratum 4 type 1 for network connected applications and type 2 for termination or standalone applications.(see Ref. #4).

SCLKx2* System clock times two -- driven by the clock master. The clock frequency is exactly twice that of SCLK. Its rising edge is defined to trigger the transitions of the SCLK and FSYNC on the clock master card. The primary purpose for this signal is to provide compatibility with ST-bus systems which need the SCLKx2* signal to clock data in from the data bus at the 75% point of the SCLK cycle.

FSYNC* Frame sync -- driven by the clock master. This signal, at SCbus rate of 2.048 M bps is one SCLKx2 clock period wide, is a negative true pulse, and occurs one-quarter SCLK period prior to the start of a frame (the first bit of the first time slot) with a period of 125 us (8 KHz). It is used to synchronize all SCSA system board time slot counters. At 4.096 M 8.192 M bps, FSYNC* is one SCLK period wide and occurs one-half SCLK period prior to the start of the frame.

SREF8K Secondary clock reference. This optional 8 Khz digital signal is driven by the standby SCbus clock master which provides backup synchronization to the SCbus. This signal can have any duty cycle as long as the period is 125 microseconds +/- 32 ppm or better or is network synchronized. The only format restriction on the SREF8K signal is a minimum high or low time of 100 nanoseconds. This signal is intended to be used by the current SCbus clock master to provide network referenced SCbus timing in the event of a network clocking failure to that master.

SD[0:15] Serial data lines that can be driven by any board in the system. However, only one board can drive the bus at any given time slot on each stream. Each signal contains 32, 64, or 128 time slots per frame when the bus operates at 2.048M Hz, 4.096M Hz, and 8.192M Hz, respectively. These signals are collectively referred to as the SD bus.

CLKFAIL Clock failure -- driven by the current clock master. During normal operation, it is driven low by the current clock master to indicate that system clock is in normal operation. If it's clock source fails, the current clock master detects this condition and releases the CLKFAIL signal which is then passively pulled to the high state indicating that a system clock failure has occurred.

SL[0:4]* (optional) slot select - driven by the backplane, these negative true binary bits represent the physical slot location(1 to 31) that a given SCSA module is installed in. If slot selection logic is included in a VME-SCSA board design these pins are resistively pulled up to Vcc. Slot location 00000b(SL0:4 unconnected) should be reserved for systems where no slot select signals are provided by the backplane.

MC (optional) Message bus(or Channel). This open collector, bit serial bus is shared by all equipped SCbus modules for intermodule communications. Modules access the message bus using the CSMA/CD(collision sense, multiple access with collision detection) method. It is edge synchronous with the SCbus SCLK but runs at a 2.048 MHz rate regardless of the SCbus rate. This signal is terminated on each SCSA compatible module in the system whether a user of the message bus or not.

1.5.4. Interface covered by this standard.

This standard defines the TDM data bus and serial message bus at the system interface illustrated by the dotted line in the generalized system block diagram of Figure 1. This figure depicts typical SCSA use in two compliant system components.

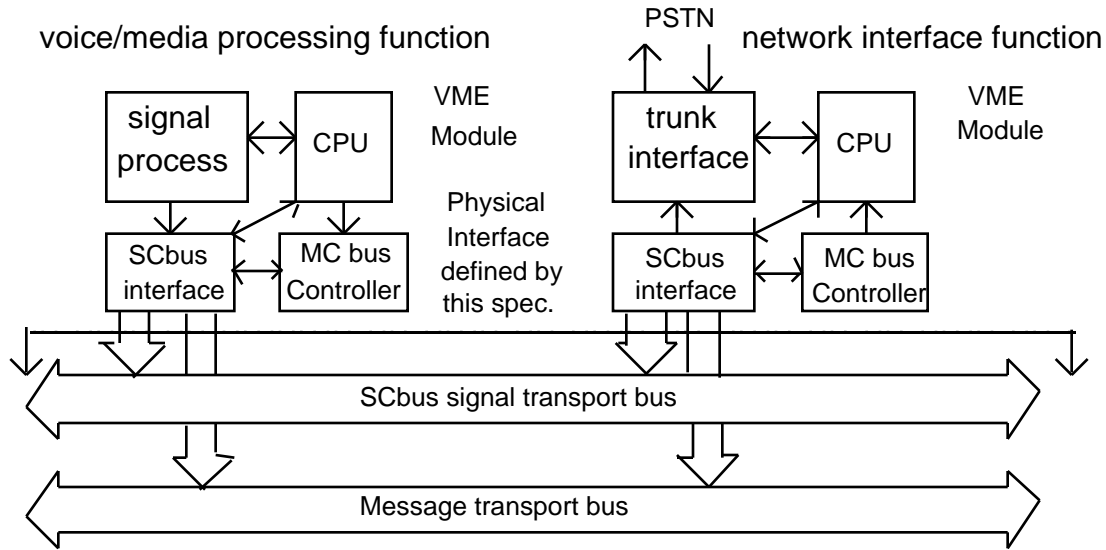


Figure 1 - Interfaces Defined by this Standard

1.5.5. System Structural Model

Figure 2 illustrates a complete VME-SCSA voice processing system node(crate) model. This model is included so that implementors may visualize the control structures that will be in place and available to service hardware/firmware products.

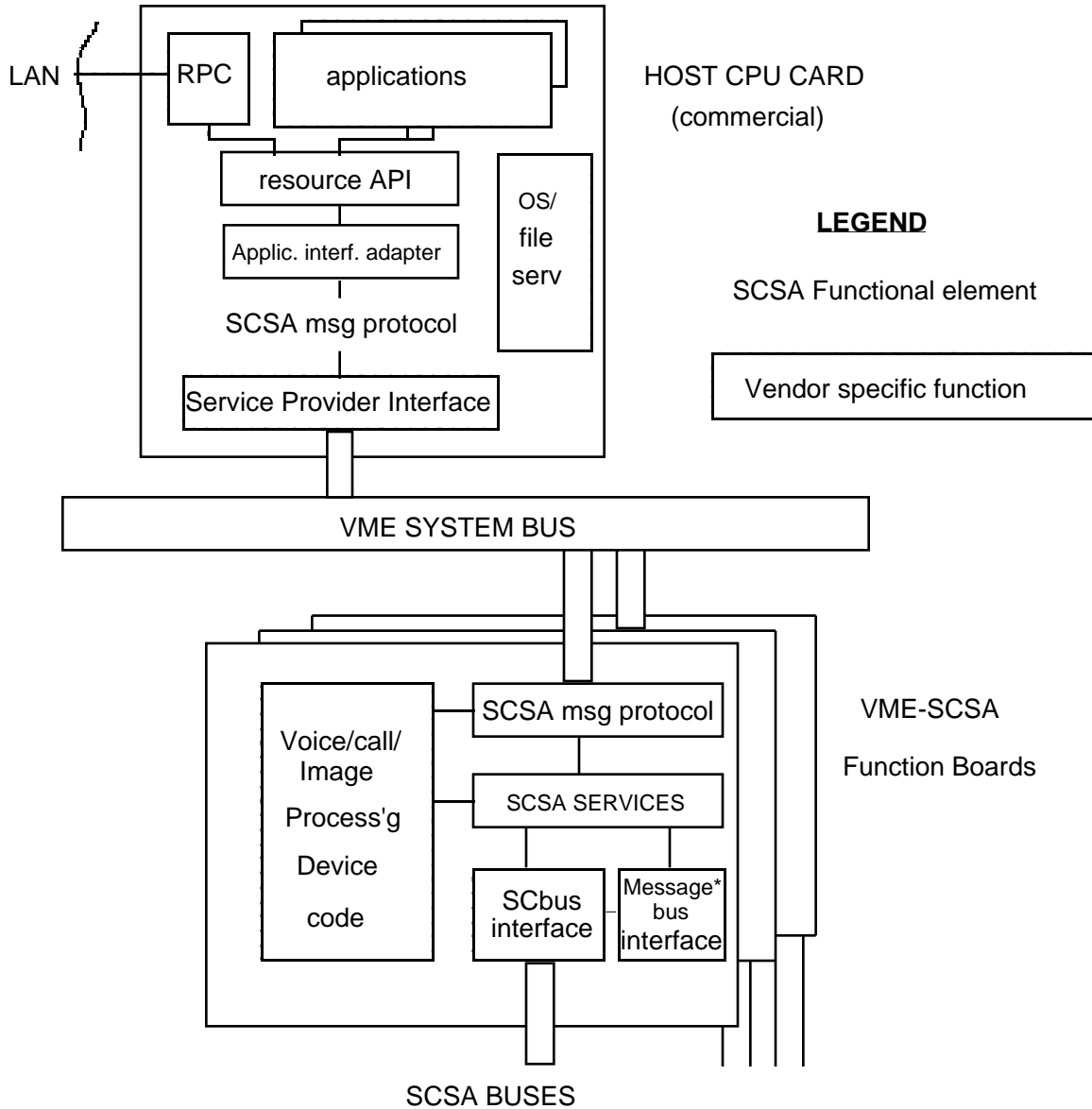


figure 2 - SCSA System Structural Model

The system elements in dotted lines in Figure 2 signify where developers will insert product specific software. The functional blocks with solid borders will become part of the separate SCSA software standard which is not system bus specific.

1.6. Specification Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this document are labeled with keywords that indicate the type of information they contain. The keywords are listed below.

RULE:
RECOMMENDATION:
SUGGESTION:
PERMISSION:
OBSERVATION:

Any text not labeled with one of these keywords describes the VME-SCSA structure or operation. It is written in either a descriptive or narrative style. These keywords are used as follows:

RULE chapter.number:

Rules form the basic framework of the VME-SCSA specification. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All SCbus or SCmessage bus rules SHALL be followed to ensure compatibility between compliant designs. Rules are characterized by an imperative style. The upper case words SHALL and SHALL NOT are reserved exclusively for stating rules in this document and are not used for any other purpose.

RECOMMENDATION chapter.number:

Wherever a recommendation appears designers would be wise to take the advice given. Doing otherwise may result in some awkward problems or poor performance. While SCSA has been designed to support high performance systems it is possible to design a system that complies with all the all the rules but has performance or reliability problems.

SUGGESTION chapter.number:

In this specification a suggestion contains advice which is helpful but not vital. The reader is urged to consider the advice given before discarding it. Some suggestions have to do with designing boards that can be easily configured or that make the job of system debugging easier.

PERMISSION chapter.number:

In some cases an SCSA rule does not specifically prohibit a certain design approach but the reader might be left wondering whether that approach might violate the spirit of the rule, or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. The upper case word MAY is reserved exclusively for stating permissions in this document and is not used for any other purpose.

OBSERVATION chapter.number

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain SCSA rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rule must be followed.

1.7. Specification Diagrams.

As aids to defining or describing SCSA bus, system or software operation several types of diagrams are used, including:

- Timing diagrams: Show the timing relationships between signal transitions. The times specified will have minimum and/or maximum limits associated with them. Some of the times included on these diagrams specify the behavior of the backplane interface logic while other times specify the interlocked behavior of the associated functional modules.
- Sequence diagrams: Show only the interlocked timing relationships of the functional modules. This diagram is intended to show a sequence of events rather than to specify the times involved.

1.8. Protocol Overview

1.8.1. Data bus

The SD data bus uses a layer one protocol and can be classified as a "best effort" bus. There is no source or destination addressing beyond the data line number, frame and timeslot location which are not module specific. The SD bus framing and clocking is as specified in section 2.1 of this document.

OBSERVATION 1.1: The connected SCbus modules avoid transmit timeslot collision only by the exclusivity guaranteed by software.

RECOMMENDATION 1.1: Robust system components should provide some means of monitoring transmissions for SCbus timeslot collisions between boards.

1.8.2. Message bus

The message bus uses a multi-layer packetized protocol whose layer two is compatible with ISO #3309(HDLC)(see ref. #6). The upper host CPU software layers and the VME function board service layers will be defined by and included in a separate document describing the SCSA software functional model and interface definitions.

CHAPTER 2

2. Data Transfer Bus

2.1. Introduction

The SC data bus is a synchronous, bit-serial, TDM transport bus operating at either 2.048M bps, 4.096M bps, or 8.192M bps. It consists of 1 or 2 clocks, 1 frame sync pulse, 16 independent, bit-serial data signals SD[0..15], and 1 clock control signal, CLKFAIL.

The VME SCbus is designed to operate at up to 8.192 MHz yielding the highest number of timeslots. The SCbus timing described in this document also provides compatibility with ISA based SCSA systems and also MITEL ST-bus based systems which operate at lower clock rates.(see section 2.6)

The clock SCLK and SCLKx2* are used to define the bit positions. The frame sync pulse FSYNC* is used to indicate the frame boundary and occurs every 125 us (8 KHz). The SD bits between the two consecutive frame pulses are divided, starting at frame boundary, into multiple 8 bit groups called time-slots. There are 32, 64, or 128 time slots in each frame depending on the bus clock speed. When SCLK is operating at 8.192M bps 128 time-slots per SD line are defined.

Table 1 shows the bus speed in Megabits/second and the resultant SD data line format with the number of time-slots per frame defined on the data bus.

Bus speed	2.048M bps	4.096M bps	8.192M bps
# of Time slots per SD per SCbus frame	32x16 = 512	64x16 = 1024	128x16 =2048
Total bandwidth	32M bps	65M bps	131M bps

Table 1 - SC Bus Speed and Capacity

The time-slot is the smallest switching unit on the bus and accounts for 64K bps of bandwidth on the SD bus.

RULE 1.1: All bus signals except SDx, MC and SREF8K SHALL be driven only by the current clock master module.

RULE 1.2: Only one board SHALL be permitted to drive a data bus serial stream during any particular time slot period or periods.

RULE 1.3: All timeslots SHALL be universal meaning that any timeslot may be used for either incoming(receive) or outgoing(transmit) data.

RULE 1.4.: Grouping multiple 8 bit timeslots to form a wide band(hyper-) channel requires switching this composite wide band channel with the same delay. That is, all grouped timeslots SHALL maintain their original position in a frame of reference and not be re-sequenced or delayed to subsequent frames. This SD bus mode SHALL be allowed and supported under this standard. Timeslot sequence SHALL be considered maintained when a set of timeslots within a frame retain their same relative positions within the frame from source to destination.

RULE 1.5: SCbus boards SHALL connect to all 16 SD signal lines to avoid excessive differential data skew on the SCbus.

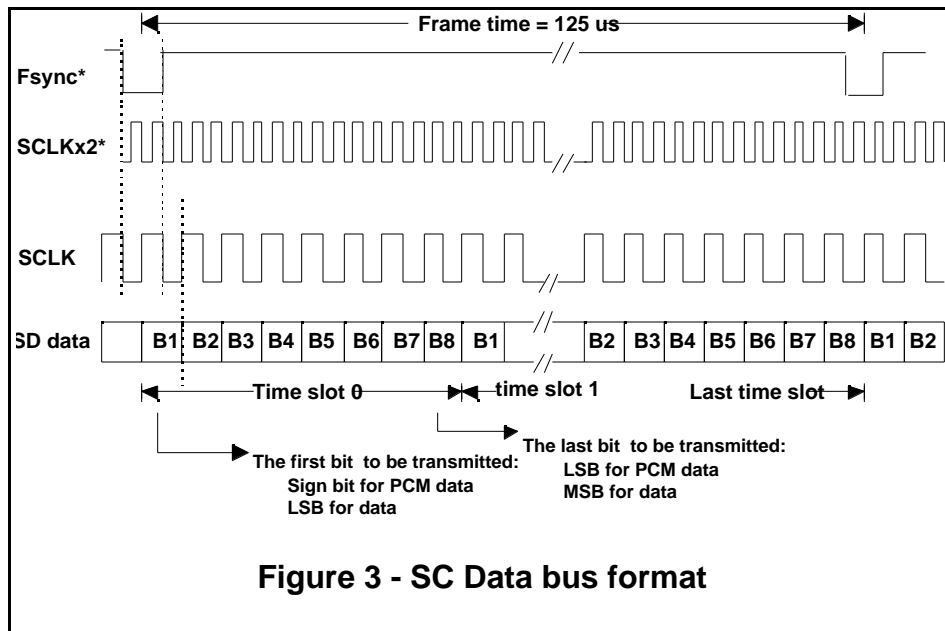
2.2. Data Transfer bus lines.

2.2.1. Bus format

Depending on the bus clock rate each SD serial stream is divided into 256, 512 or 1024 bit groups called a frame. Each frame is exactly 125 microseconds long. Each frame is then further divided, starting at the frame boundary, into a fixed number of 8 bit sub-frames called time-slots. Each frame consists of 32, 64, or 128 time slots corresponding to the respective clock rates of 2.048, 4.096 or 8.192 MHz.. The first 8 bit group following a frame sync is designated as TS0 (time-slot 0); the second 8 bit group is TS1 (time-slot 1) and so on. The first bit in each time-slot is designated as B1 and is transmitted or received first. The last bit in the timeslot is designated as B8 and is transmitted or received last.

This timeslot bit identification adheres to the ITU-T G.711 convention for PCM encoded voice samples where B1 is the sign bit and B2 is the MSB of the PCM code word. For clear channel data applications, B1 is the LSB of the data code word.

RULE 2.1: Digit or bit sequence integrity SHALL be maintained for the length of the transmission path. Bit integrity SHALL be considered to be maintained when the binary values within an octet are exactly reproduced at the receiver.



Notes: The pictorial presentation of bit positions varies among different documents. B1 is at the right most position in Q.921/Q.931 ISDN recommendation whereas it is at the left most position in G.711 voice telephony recommendation. Therefore, always use the bit designation from the appropriate reference source.

2.2.2. Frame alignment

The relationship between data, clock, and frame pulse is also illustrated in diagram of Figure 3. Refer to section 2.4 of this document for detailed SCbus timing information.

2.2.3. Bearer channel levels on the SCbus

2.2.3.1. Telephonic Voice Channels

RECOMMENDATION 2.1: The format for binary coded and companded 3.1 KHz bandwidth digital voice data on the SCbus should be restricted to either mu-law PCM or A-law PCM, as defined by ITU-T G.703.

It is undesirable for digital network interface boards to modify encoded analog timeslot content. Therefore, the average encoded speech energy level impressed on an SCbus time slot by a resource module for network transmission should not exceed -12 dbm0 when averaged over any 3-second period. This results in a TLP 0 system level point on the SCbus. For analog network systems to be installed in the US, the average encoded speech energy level impressed on an SCbus time slot by a resource module should not exceed -9 dbm0 when averaged over 3-second period. This assumes a PCM to analog decode level of zero(0 DL).

OBSERVATION 2.1: The permitted levels for tone addressing(DTMF) and signaling are normally higher than allowed voice levels. The appropriate network standards should be consulted before establishing transmission levels for tone signaling.

RECOMMENDATION 2.2: Always check the national network limits before assuming that any stated levels are correct. Resource modules are usually responsible for controlling network transmission levels in SCSA systems.

2.2.3.2. Other Media Data Streams

The timeslot content for non-telephonic voice applications is not restricted for the purpose of this standard.

2.3. Operation

2.3.1. Synchronization

There are three types of synchronization; bit, time-slot, and frame. Bit synchronization establishes proper timing to send and/or receive data bits. Time-slot and frame synchronization ensure that each board operation is synchronized with the other boards within the system. Since the operation of the bus does not require any handshake between a sender and the receiver(s), the synchronization is crucial to the system operation (see section 2.3.2 and 2.4. for details). The following rules apply to all compliant boards used in a SCbus system:

RULE 2.2: Data SHALL be sent to the SCbus on the rising edge of the SCLK.

RULE 2.3: Data SHALL be sampled on the SCbus at or after the falling edge of SCLK.

RULE 2.4: Timeslot counters SHALL use the rising edge of SCLK to increment or reset the counter.

RULE 2.5: Timeslot counters SHALL be reset to zero at the rising edge of SCLK coincident with the FSYNC* frame sync pulse.

2.3.2. Voice/data Transfers

SCbus is a bit-serial, synchronous, TDM transport bus. Voice/data transfer on the bus is accomplished by assigning one or more time-slot IDs (an SD_n bus stream number plus a time-slot number) to the sender and receiver. At the selected time-slot, the sender drives the bus and the receiver clocks-in the data bits. There will be no handshake or confirmation taking place between the sender and the receiver(s). The operation is solely based on the assumption that all boards in the system use the SCLK and have their time-slot counters synchronized to the frame sync pulse.

RECOMMENDATION 2.3: Some means should be employed to detect or prevent collisions caused by two resources attempting to transmit on the same SCbus timeslot. Collision detection may be employed either continuously or periodically. Alternatively, prior to transmitting on a timeslot, a resource may first "listen" to the intended timeslot for the all "ones" FFH pattern resulting from all bits being pulled up by the SCbus terminators.

SCbus architecture supports three types of data transfer. The following definitions are repeated to facilitate the subsequent discussions;

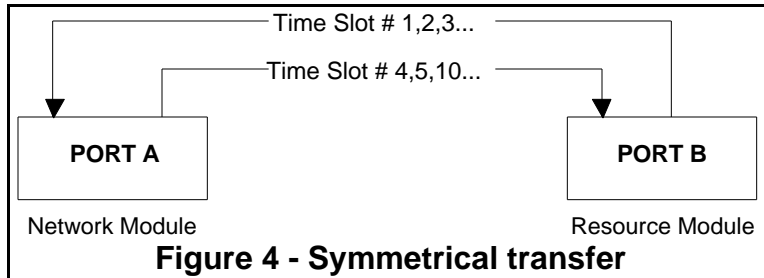
-Channel: Is a transmission path that transports information from one end point to the other. Channel capacity is not limited to one time slot.

-Port: In the context of this document, a port is an interface point where an external communication channel is terminated and information is exchanged.

-Call: A call exists when an SCbus channel is assigned to a telephony port in the seized or connected network state.

2.3.2.1. Symmetrical Transfer

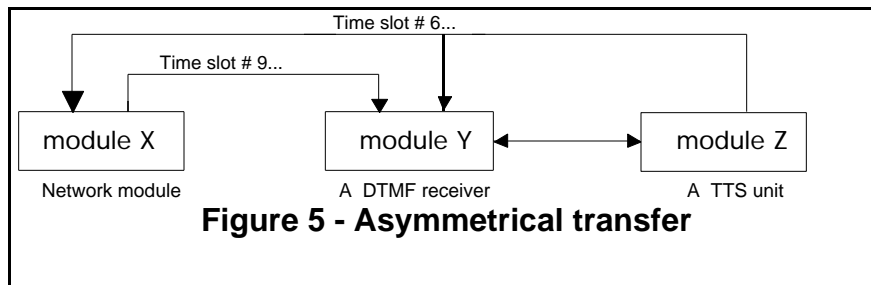
Symmetrical transfer is a transfer mode by which a pair of SCbus modules communicates with each other forming a full duplex path.



In this example, port A uses time slots 4,5, and 10 to send data to port B. Port B uses time slots 1,2, and 3 to send data to port A. This transfer mode is used in most applications. In an example system environment, port A can be a network module and port B a resource module.

2.3.2.2. Asymmetrical Transfer

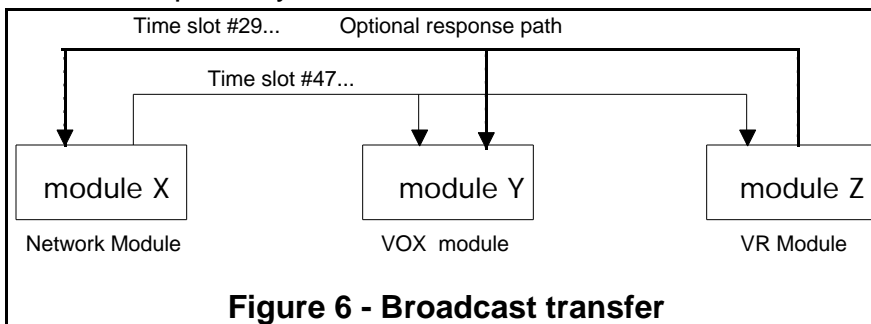
Asymmetrical transfer is an SCbus transfer mode by which the transmitting module receives data from a module other than the module it sends data to:



In Figure #5, module X uses time slot 9 to send data to module Y and time slot 6 to receive data sent from module Z. In this example, module Y can optionally receive data from module Z on time slot 6.

2.3.2.3. Broadcasting

This is an SCbus transfer mode by which one module can send data to multiple channels simultaneously. In Figure # 6, module X sends data on time slot 47 to module Y and Z. Module Y can optionally receive data from module Z.



OBSERVATION 2.3: Broadcast mode is necessary for applications such as music-on-hold, video or audio conferencing.

2.4. SCbus Clocking Considerations

In systems connected to the public switched telephone network, synchronization must be maintained under all conditions. High availability systems are expected to provide redundant sources of network synchronized clock. Clock fallback provides for the orderly transition of SCbus clocking to a backup clock master.

2.4.1. SCbus Clock Agents

RULE 2.6: SCbus modules SHALL assume one of the following identities with respect to SCbus clocking:

(a) Clock Slave: An SCbus agent or module which receives the SCbus timing signals SCLK, SCLKx2* and FSYNC* for use in transferring data on the SCbus SD lines.

(b) Clock Master: An SCbus agent or module which is capable of assuming SCbus mastership by properly driving the SCbus timing signals. SCbus masters SHALL have the following capabilities:

- Be capable of driving the SCbus timing signals SCLK, SCLKx2* and FSYNC*.
- Be capable of also operating as an SCbus clock slave.
- Be able to detect when SCbus clocking or timing has failed and be able to notify the system host.
- Be able to detect when it's own synchronization or SCbus timing drive circuits have failed and be armed to release the CLKFAIL signal and cease driving the SCbus clocks and frame sync.
- Be able to be armed as an SCbus standby clock master which assumes SCbus mastership if and when the SCbus CLKFAIL signal becomes active(true).
- Be able to supply an accurate internal clock reference source(suggest +/- 32 ppm) from which to derive SCbus timing for system boot-up or for non-network connected installations.

RULE 2.7: If SREF8K mode is supported, clock master modules SHALL provide:

-SREF8K Slave capability: modules must monitor signal presence on SCbus signal SREF8K and synchronize it's SCLK clock reference circuits to SREF8K when enabled under host or internal module control.

-(Optional)SREF8K Master capability: modules must derive an 8 KHz reference signal from it's network synchronization circuits or from an internal clock reference and then drive SCbus signal SREF8K when enabled under host or internal control.

-The SCbus electrical load(slave) and drive(master) requirements specified in table 9 also apply to SREF8K interface circuits.

2.4.2. Clock Fallback

Clock fallback is a procedure by which a different physical source of network synchronized clock is provided for the SCSA application system. This procedure involves organizing all boards that can drive network synchronized clocking signals to SCbus into a clock fallback hierarchy. Each subsequent standby clock module in the hierarchy is first enabled by software to become the new SCbus clock master if it's immediate superior fails. The actual clock mastership transfer should be hardware initiated(by CLKFAIL) as a normal mode of operation.

When implemented, clock fallback occurs under hardware control when:
-CLKFAIL SCbus signal is no longer held low by the current clock master, or
-clock irregularity is detected on the bus.

Clock irregularity is defined as the existence of one or more of the following conditions:

- SCLK, or SCLKx2* or FSYNC* disappears from the SCbus for more than a designated period, typically one frame.

- FSYNC* and SCLK are out of synchronization (an incorrect number of clock counts between two frame pulses).

RULE 2.8: The CLKFAIL signal SHALL be released by the current clock master when it's own faulty clocking is detected or when requested by system software. The latter is an explicit request for clock switch over.

RULE 2.9: If the persistent absence of a clock signal or FSYNC* is not detected by the current clock master it SHALL be detected by the next standby clock module in the fallback hierarchy.

This condition is considered a major system alarm and needs to be reported to the host CPU by the standby clock module.

RULE 2.10: If the standby clock module has not reported the resumption of bus clocking after a period not to exceed sixty(60) milliseconds the host CPU software SHALL explicitly request that the original clock master stop driving the clocks, FSYNC* and CLKFAIL bus signals by all means available.

RULE 2.11: A reliable hardware and software mechanism SHALL be provided to unconditionally cause the current clock master module to release the CLKFAIL signal and to stop driving the bus timing signals to allow the standby clock master to assume bus clocking responsibility.

RULE 2.12: Clock master modules SHALL provide a means to automatically become a clock slave in the event that it either: (a)detects a failure of it's clock generating circuitry, initiates release of CLKFAIL and stops driving the SCbus timing signals, or, (b)is commanded by the host CPU to release CLKFAIL and to stop driving the SCbus timing signals.

2.4.2.1. Clock fallback List.

As described above, the SCbus provides the hardware mechanism by which the current clock master relinquishes clocking responsibility to a standby clock source. However, the SCbus directly provides for only a primary and a secondary(standby) clock master at one time. If a given system contains more than two potential synchronized clock sources prudent system design dictates that all should be included in an SCbus clocking hierarchy. The host CPU based device software is usually responsible for implementing a multi-level clock fallback strategy.

RECOMMENDATION 2.4: SCSA systems should implement a clock fallback list. The recommended method for administrating a clock master hierarchy is via a clock fallback list. The clock fallback list is an ordered list of the identification (ID) of the boards that can be used as clock masters. The board ID scheme and the size of the fallback list are two system variables under the control of the system developer. Since physical telephony trunks are associated with particular VME shelf slot numbers it is suggested that the SCbus backplane-provided slot ID be included in the board ID.

OBSERVATION 2.4: There needs to be at least one valid entry (ID) in the list in order to make system operational (the SCbus needs a timing source to operate).

To be a valid clock source, a network board needs to: 1) be able to generate or derive clock and frame sync, and 2) the bus drivers need to meet the electrical requirements specified in chapter 5 of this document

After power is initially applied and prior to the completion of system initialization, host CPU software needs to designate a board capable of providing both clocks and FSYNC* as the SCbus clock master in order to keep the SCbus and message bus operational until such time that the primary clock source on the fallback list becomes available and becomes synchronized to the network.

If there is more than one entry on the clock hierarchy, the first entry is designated as the current clock master and the second entry is the standby clock master. While the system is running, the host CPU should have the ability to change the current clock master by software command.

When the clock master is changed for any reason, the next clock source in the list needs to be designated as the next standby master by the host CPU software.

2.4.2.2. Clock fallback Timer.

RECOMMENDATION 2.5: SCSA systems should implement a clock fallback timer. A clock-fallback timer is a system parameter that is used to prevent the SCbus operation from being locked up due to a clock master board failure. This timer needs to be implemented by the device software on the host CPU and by standby clock master modules.

As mentioned above, when the current clock master releases CLKFAIL it must also notify the host CPU. The host CPU software starts and monitors this timer until the standby clock master reports that it has assumed SCbus clock mastership and has pulled down CLKFAIL. If the timer expires, the host CPU software must attempt to reassign the current(non-responding) clock standby board as a clock slave and then select another clock source board from the fallback list as the next clock master. Subsequently, a new standby master should be designated, if available.

A similar timer should also be implemented by the clock standby module to monitor the clock activity on the SCbus. Should a reported clock irregularity condition persist beyond the timer period, the designated standby module must report the status of the clocks and CLKFAIL signal to the host CPU which can then reassign clock mastership as above.

A suggested maximum value for the host timer is 60 ms. That is, the standby clock master is allowed to be delayed up to 60 ms in pulling down CLKFAIL after it is released by the original master. The value of the standby module timer should be shorter than the host value(see **RULE 2.15**).

2.4.2.3. CLKFAIL Procedure

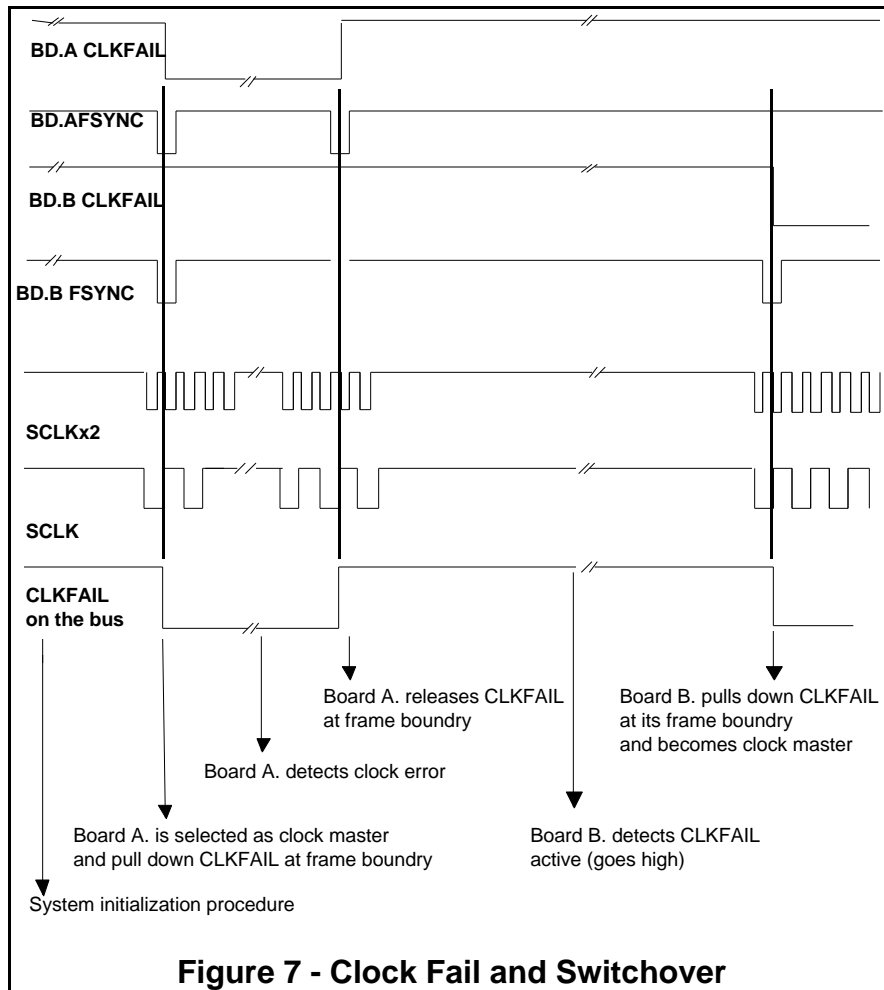
The detailed protocol for the CLKFAIL event is described in Table 2.

Normal operation	<ol style="list-style-type: none"> 1. Clock master provides clocks and frame sync pulse
After clock source error is detected by the clock master or per the system host CPU software request	<ol style="list-style-type: none"> 1. Clock master continues to provide clocks until the next frame pulse time if possible. 2. At the next frame pulse time, the clock master releases CLKFAIL and runs clocks one more cycle then releases the clock (clocks revert to high state). 3. After clocks are released, the current clock master disarms itself to prevent fallback oscillation.
If clock irregularity is detected by the standby module	<ol style="list-style-type: none"> 1. The standby master reports status to the host CPU software which starts the timer. If the condition persists when the timer expires, the host CPU software begins manual clock switchover.
Switching over	<ol style="list-style-type: none"> 1. After CLKFAIL is released, the standby board prepares to drive SCLK and SCLKx2 and pulls down CLKFAIL at the falling edge of the next standby-board-generated FSYNC. 2. The standby board begins to supply bus clocks. 3. The new clock master delays its' first frame pulse to the next frame pulse. After the clock is switched over, the host CPU software selects and enables a new standby clock master.

Table 2 - Clock Fail Fallback Procedure

2.4.2.4. Clock Fallback Scenario

The following scenario illustrates the sequence of events after CLKFAIL becomes active;



OBSERVATION 2.4: When clock irregularity occurs, turning off the clock master may not be as graceful as shown above. However, the clock turn-on sequence needs to follow the sequence as shown above.

2.4.2.5. System Recovery Performance Requirements

To provide standardized response to network carrier or clock module failure the following are to be implemented at system level:

RULE 2.13:: The clock master exchange process SHALL be completed in all cases within 100 ms after clock error or failure occurs.

OBSERVATION 2.5: When network clocking fails it is assumed that the phase locked loop(PLL) used to recover the clock on the clock master module will continue to generate the SCbus clock signals. The PLL will slowly drift off frequency until the clock master switches to SREF8K synchronization(if supported) or the host CPU deselects the current clock master and allows the standby clock master to assume mastership of the SCbus. If a failure of any of the current clock master SCbus drive circuits occurs, the master is obligated to stop driving the SCbus and CLKFAIL as soon as it detects the failure. An SCSA compliant standby clock master will detect the failure within a few microseconds and seize SCbus mastership. SCbus operation will then resume.

RECOMMENDATION 2.6: SCbus digital network interface modules should include a phase-locked loop(PLL) between the SCbus clock and it's transmitting circuits to prevent discontinuities in the transmit bit stream to the network(ref. ANSI T1.101-1987 section 6.6). SCbus clock gaps that occur during bus clock master switchover will be "bridged" by the PLL.

RECOMMENDATION 2.7: As during clock switchover, any time that no clocks are present on the SCbus the content of the SD lines is indeterminate possibly causing undesirable transmitted network codes. It is recommended that after the signaling "freeze" period(see rule 2.14) and if the CLKFAIL signal is active(high) that all "ones"(T1 "blue alarm") be transmitted to the network or else an appropriate alarm pattern for the network of installation.

RULE 2.14: During the clock switchover period, channel-associated(i.e. T1 "robbed bit" or E1 "ABCD") trunk signaling in the transmit direction SHALL be frozen in the current state until SCbus clock returns or until a maximum of one second of CLKFAIL high time.

RULE 2.15: The designated clock standby module SHALL be able to determine the quality of the system clock, and report to the host when any clocking irregularity persists for longer than 20 ms.

2.4.3. Initialization

2.4.3.1. SD bus

RULE 2.16: When the power is initially turned on, all boards SHALL disable their SCbus drivers until system initialization procedure is completed. Unless a timeslot number has been pre-assigned by the system software, SCbus boards SHALL NOT drive the bus.

2.4.3.2. Clocks and Frame Sync Pulse.

When the power is initially applied, these signal lines float "high" due to the bus terminators until a system board is designated as the system clock master, either by a software command or the clock-fallback mechanism. The system clock initialization sequence is listed in Table 3.

OBSERVATION 2.6: The system-wide clock failure detection and fallback functions

1	When power is initially applied, the clock fallback circuit on each clock source board is disabled.
2	Clock source boards within the system monitor the status of the clock or CLKFAIL. If clocks are present on the bus or CLKFAIL is pulled low, these boards will consider themselves as SCbus clock slaves.
3	A board may be selected as clock master prior to the presence of network derived clocks by a software command. The purpose of this action is to let the system start up during the initialization procedure. This clock master is called boot master and could be any board capable of driving the clocks and FSYNC and need not be listed on the fallback list.
4	Until at least one listed clock source board reports back its active clock status (after the initialization procedure), the system administrator can not select a clock master.
5	The designated clock master drives the system clocks and FSYNC and pulls down the CLKFAIL signal.
6	Only after the clock master pulls CLKFAIL low and reports valid clock status shall the system administrator enable another clock source to be the standby clock master.

Table 3 - Clock Initialization Procedure

need to initially be turned off to allow the system to be downloaded and stabilized

2.4.4. Unused timeslots

RULE 2.17: All unused time-slots SHALL be left undriven by all boards so that the data bus can be pulled to the high state by the SCbus terminators.

2.5. Data Transfer Modules - Basic Description

VME bus modules that connect to the SC data bus are expected to maintain synchronization with the SCbus and utilize the SD signals and timeslots to receive as well as drive byte oriented data onto the bus. Since there is no addressing of the bus data these operations take place under the control of the SCSA switching and resource management software.

PERMISSION 2.2: Multiple SC data bus timeslots, up to an entire frame, may be used for any desired transfer operation. There are no content formatting requirements for timeslots or groups of timeslots (called hyperchannels) as long as the source and destination modules are aware of the formatting.

RECOMMENDATION 2.8: Unless a comprehensive, system-wide level plan is implemented SCbus modules which exchange PCM encoded telephonic voice signals with the SCbus and which are ultimately destined for the switched public network, should assume or adjust signal levels to a transmission level point (TLP) of zero when receiving or sending PCM information to the SCbus.

2.6. Typical Operation.

The SCbus is designed to operate in one of three modes.

- In pure VME SCSA systems with terminated PCB backplanes the bus is clocked at 8.192 MHz providing the maximum number of SCbus timeslots.
- In mixed VME-ISA bus systems or when ribbon cable is used to connect the SCbuses, SCLK is reduced to 4.096 MHz and the ribbon is unterminated.
- In systems containing ST-bus compatible modules SCLK is reduced to 2.048 MHz, SCLK*2 is required and the ribbon is unterminated.

The SCbus timing for these rates is in the following sections.

2.6.1. Data Transfer Bus Modules - Timing Rules and Observations

All SCbus timing parameters refer to Figure 8 below. All receiver related timings are backplane worst case that include allowances for skew, propagation delay and rise time plus margins.

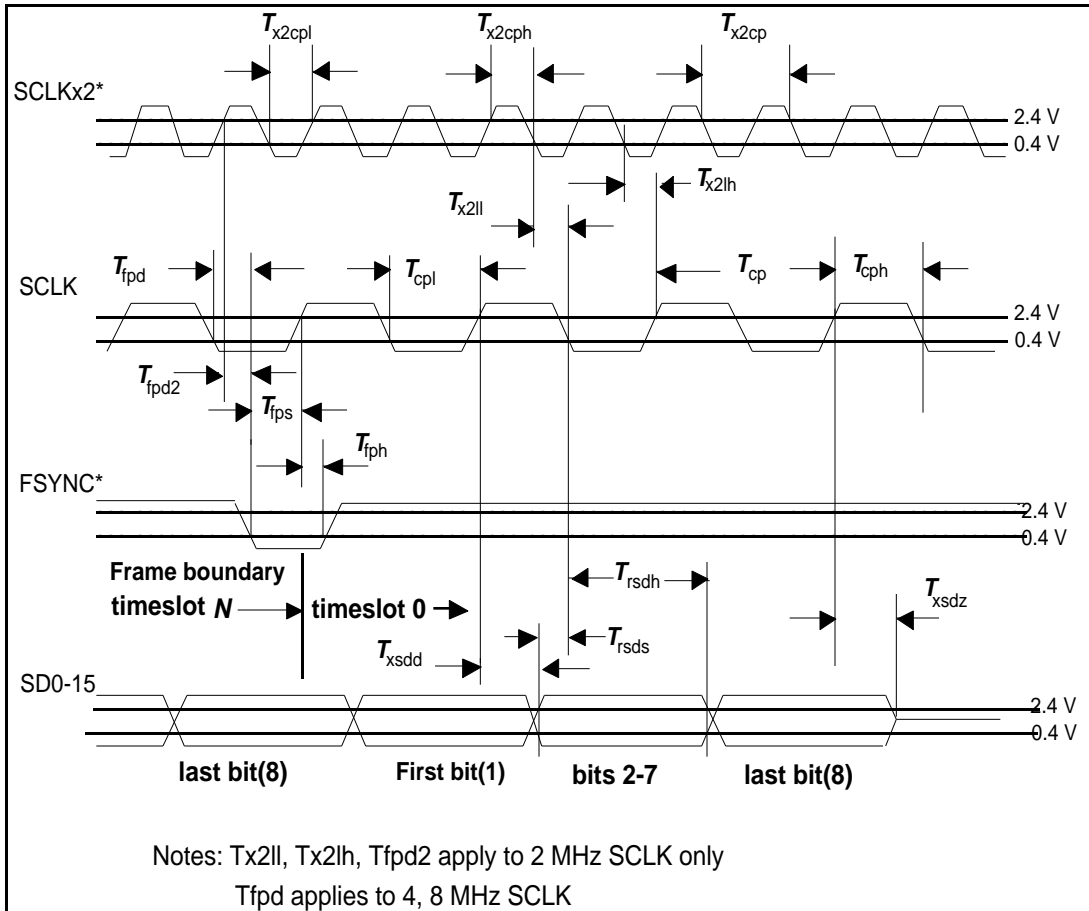


Figure 8 - Detailed Data bus Timing

2.6.1.1. Data Bus Timing at Bus Speed = 2.048 M Hz

Referring to Figure 8, a 2.048 M Hz implementation of the SCbus should have the timing specified in Table 4:

Symbol	Descriptions	Min	Typical	Max	Unit
T x2cph	Clock period high at 4.096M Hz	115	122	130	ns
T x2cpl	Clock period low at 4.096M Hz	115	122	130	ns
T x2cp	Clock period at 4.096M Hz	241	244	247	ns
T cph	Clock period high at 2.048M Hz	237	244	252	ns
T cpl	Clock period low at 2.048M Hz	237	244	252	ns
T cp	Clock period at 2.048M Hz	483	488	493	ns
T x2ll	4M clock low to 2M clock low delay	-10		10	ns
T x2lh	4M clock low to 2M clock high delay	-10		10	ns
T fpd2	Frame pulse delay -- from the SCLKx2 clock going high to valid output on the bus. A specification for the transmitter.	-10		25	ns
T fps	Frame pulse set up time -- from valid FSYNC* to the rising edge of SCLK. A specification for the receiver.	15			ns
T fph	Frame sync pulse hold -- valid FSYNC* after the rising edge of SCLK. A specification for the receiver.	10			ns
T xsdd	Output data delay -- from the rising edge of SCLK to valid output or output enabled on the bus. A specification for the transmitter.	30		90	ns
T rsds	Input data set up time -- from valid data to the next falling edge of SCLK. A specification for the receiver.	25			ns
T rsdh	Input data hold time -- valid data after the falling edge of SCLK. A specification for the receiver.	30			ns
T xsdz	Output disable delay-- from the SCLK rising edge to output disabled. A specification for the transmitter.	0		20	ns

Table 4 - Data Bus Timing at 2.048 M Hz bus speed

2.6.1.2. Data Bus Timing at Bus Speed = 4.096M Hz

Referring to Figure 8, a 4.096 M Hz implementation of the SCbus should have the timing specified in Table 5:

Symbol	Descriptions	Min	Typical	Max	Unit
T x2cph	Clock period high at 8.192M Hz(see note below)	55	61	67	ns
T x2cpl	Clock period low at 8.192M Hz(see note below)	55	61	67	ns
T x2cp	Clock period at 8.192M Hz(see note below)	120	122	124	ns
T cph	Clock period high at 4.096M Hz	115	122	130	ns
T cpl	Clock period low at 4.096M Hz	115	122	130	ns
T cp	Clock period at 4.096M Hz	241	244	247	ns
T fpd	Frame pulse delay -- from the falling edge of SCLK to valid output on the bus. A specification for the transmitter.	-10		90	ns
T fps	Frame pulse set up time -- from valid FSYNC* to the rising edge of SCLK. A specification for the receiver.	15			ns
T fph	Frame sync pulse hold -- valid FSYNC* after the rising edge of SCLK. A specification for the receiver.	30			ns
T xsdd	Output data delay -- from the rising edge of SCLK to valid output or output enabled on the bus. A specification for the transmitter.	30		60	ns
T rsds	Input data set up time -- from valid data to the next falling edge of SCLK. A specification for the receiver.	25			ns
T rsdh	Input data hold time -- valid data after the falling edge of SCLK. A specification for the receiver.	30			ns
T xsdz	Output disable delay-- from the rising edge of SCLK to any output disabled. A specification for the transmitter.	0		20	ns

Note: SCLK*2 optional and not referenced to SCbus timing at this bus speed.

Table 5 - Data Bus Timing at Bus Speed of 4.096 M Hz

2.6.1.3. Data Bus Timing at Bus Speed = 8.192M Hz

Referring to Figure 8, a 8.192 M Hz implementation of the SCbus should have the timing specified in Table 6:

Symbol	Description	Min	Typical	Max	Unit
T x2cph	Clock period high at 16.384M Hz(see note below)	26	31	35	ns
T x2cpl	Clock period low at 16.384M Hz (see note below)	26	31	35	ns
T x2cp	Clock period at 16.384M Hz (see note below)	59	61	63	ns
T cph	Clock period high at 8.192M Hz	55	61	67	ns
T cpl	Clock period low at 8.192M Hz	55	61	67	ns
T cp	Clock period at 8.192M Hz	120	122	124	ns
T fpd	Frame pulse delay -- from the falling edge of SCLK clock to valid output on the bus. A specification for the transmitter.	-10		25	ns
T fps	Frame pulse set up time -- from valid FSYNC* to the rising edge of SCLK. A specification for the receiver.	10			ns
T fph	Frame sync pulse hold -- valid FSYNC* after the rising edge of SCLK. A specification for the receiver.	30			ns
T xsdd	Output data delay -- from the rising edge of SCLK to valid output or output enabled on the bus. A specification for the transmitter.	15		38	ns
T rsds	Input data set up time -- from valid data to the next falling edge of SCLK. A specification for the receiver.	10			ns
T rsdh	Input data hold time -- valid data after the falling edge of SCLK. A specification for the receiver.	30			ns
T xsdz	Output disable delay-- from the SCLK rising edge to output disabled. A specification for the transmitter.	0		8	ns

Note: SCLK*2 optional and not referenced to SCbus timing at this bus speed.

Table 6 - Data Bus Timing at Bus Speed of 8.192 M Hz

2.6.1.4 SREF8K timing

RECOMMENDATION 2.9: The optional SREF8K signal is intended as a backup synchronization resource line for clock master modules with or without a network interface. It should be driven by only one module at a time which is also not the current SCbus clock master. The SREF8K signal timing should be as follows:

- Period: 125 microseconds, network synchronized or +/- 32 ppm maximum error.
- Pulse high or low time: 100 nanoseconds minimum.

CHAPTER 3

3. Message Bus

3.1. Introduction

SCSA also provides a secondary communication medium. It is provided to support low latency and high priority inter-board and -chassis messages. This channel uses a single wire serial bus called the message bus. The message bus operates in a collision sense, multiple access with collision detection(CSMA/CD) access mode. The information transported on the bus is in packet format using the ISO #3309 (HDLC) structure(see ref. #6).

3.2. Message Bus Lines

3.2.1. Signal Definition

3.2.1.1. MC - Message bus

This line contains bit-serial, logical true, RZ data and is driven with an open collector driver. Data is shifted onto this line with a 2.048M Hz clock, referred to as MC clock.(see Figure 9).

OBSERVATION 3.1: MC clock **IS NOT** available on the SCbus, and needs to be generated on every board that intends to use the message bus.

3.2.1.2. MC Clock

MC clock is used for transmission, reception and collision detection. The relationships among SCLK, FSYNC, MC and MC clock are shown in Figure 9.

RULE 3.1: MC clock SHALL always be 2.048 MHz regardless of the SCbus SCLK clock rate.

RULE 3.2: Serial data SHALL be put onto signal MC on the rising edge of MC clock.

RULE 3.3: Serial data SHALL be sampled on MC on the falling edge of MC clock.

RECOMMENDATION 3.1: MC clock falling edge should be offset from 50:50 symmetry to provide extended MC data setup time for the message bus controller. This clock timing also provides rejection of crosstalk from the SD lines to signal MC that may occur when using ribbon cable for the SCbus.

Figure 9 shows the recommended relationship between MC clock and SCLK at all SCbus rates. The detailed MC clock timing is covered in figure 14 and table 7.

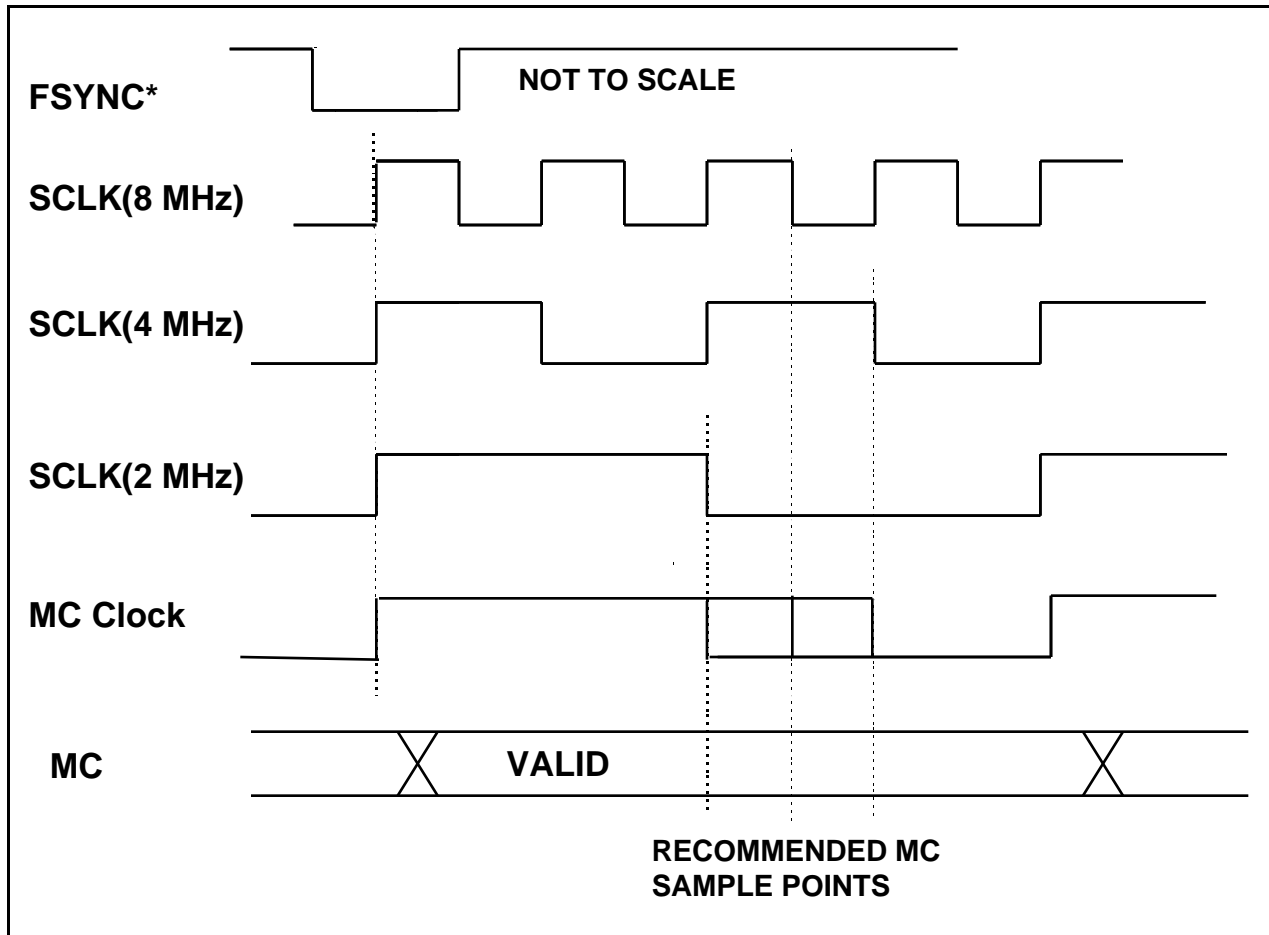


Figure 9

Relationship between FSYNC*, SCLK, and MC clock

OBSERVATION 3.2: The MC clock alignment to frame sync shown in figure 9 guarantees that all message bus agents are phase-synchronized. This condition is necessary to permit reliable collision detection between message bus modules.

OBSERVATION 3.3: MC clock is always 2.048M bps. Therefore, each message bus module should use a programmable divider for the MC clock generator to provide maximum flexibility of SCbus rates.

3.2.2. MC Signal Format

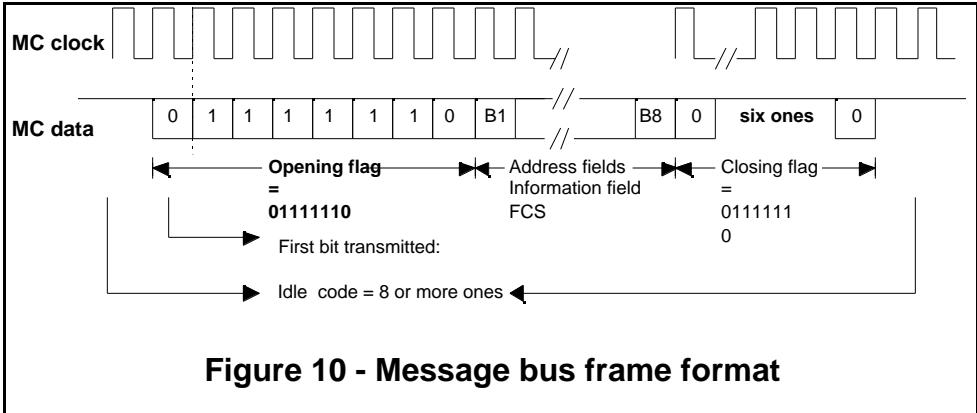
3.2.2.1. Idle

RULE 3.4: Even when the message bus is not used, signal MC SHALL be pulled high by a resistor(see section 3.6.2). When there are more than 8 consecutive 1's on the bus, the bus SHALL be considered to be in 'IDLE' state.

OBSERVATION 3.5: The message bus signal MC 'bus idle' code may be different from the PCM "idle" code on voice encoded digital trunks.

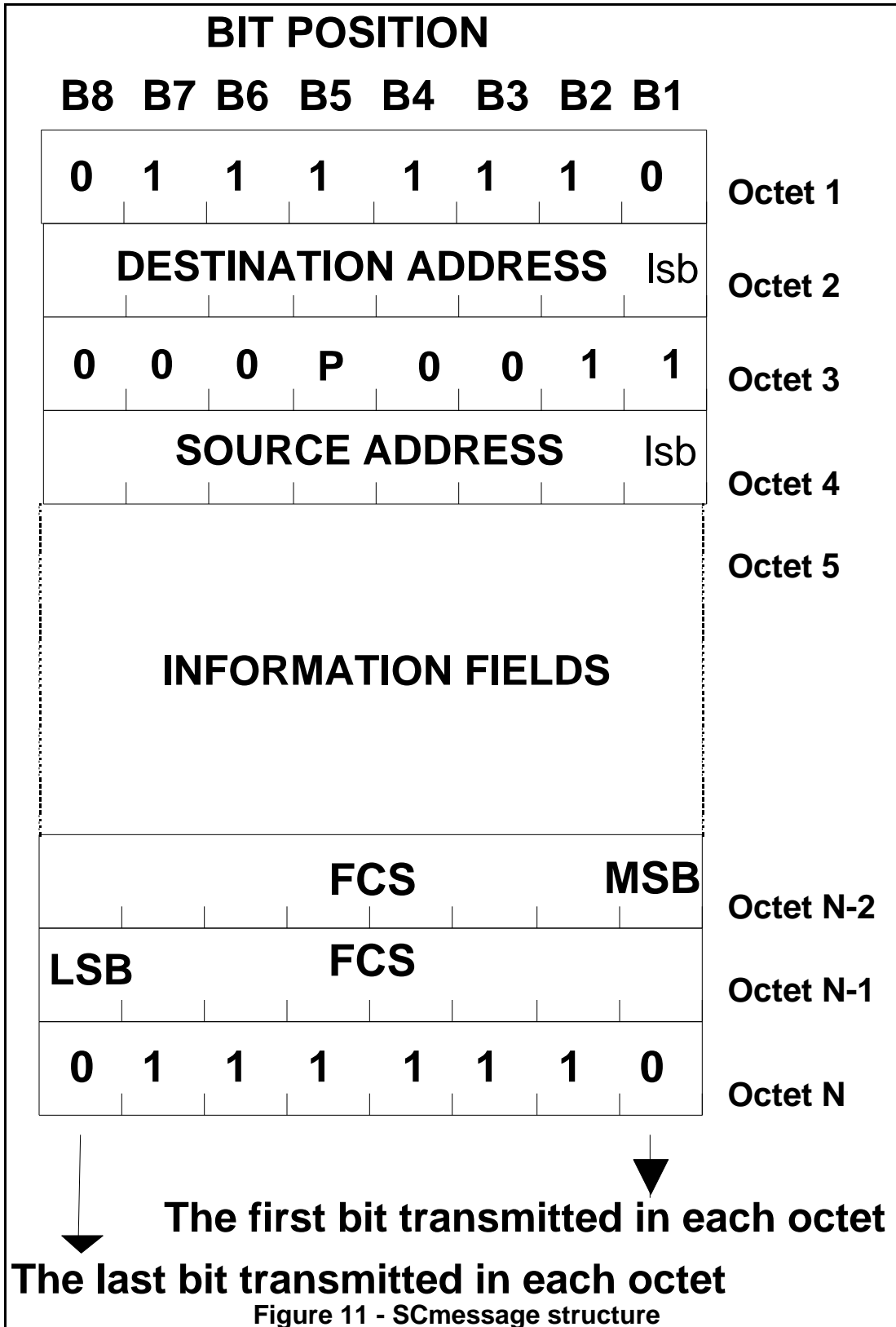
3.2.2.2. Frame Format

The message format on the message bus is frame based. Each frame is encapsulated by a pair of HDLC flags (01111110b)(see ref. #6). The first four octets of the frame are used for data link layer control. The last two octets are the frame check sequence (FCS) also used by the data link layer.



3.2.2.3. MC Message Structure

Messages sent over the message bus should adhere to the structure detailed in Figure 11.



3.3. Message Bus Field Structure

RULE 3.6: The field definitions in this section SHALL be adhered to in order to provide data link compatibility between vendors.

3.3.1. Octet 1 - Initial Flag

Per HDLC (ref. # 6), hex 7E or binary 0111 1110b.

3.3.2. Octet 2 - Destination Address

The content of octet 2 varies depending on the message type.

(a) *Point-to-Point Message:* Messages sent to a single destination must have Octet 2 containing the binary equivalent of the decimal destination node ID number, from 1 to 31 or 0000 0001b to 0001 1111b.

(b) *Broadcast Message:* Messages sent to all nodes on the local message bus must have octet 2 containing decimal destination node ID number of 255 or 1111 1111b.

Note: Broadcast messages must not cause an automatic acknowledgment from receiving nodes. However, the sending node should set the Poll bit in octet 3 to zero(see section 3.3.3).

3.3.3. Octet 3 - Control

For all SCSA compatible nodes the content of octet 4 must be as follows:

B8	B7	B6	B5	B4	B3	B2	B1
R(0)	R(0)	R(0)	P	R(0)	R(0)	R(1)	R(1)

Figure 12 Message Bus Frame Control octet

Notes:

R(0) = Reserved - set to zero.

R(1) = Reserved - set to one.

P = poll bit. Used to request or suppress receiver response.

For P = 1, receiving node must provide a response message.

For P = 0, receiving node should not automatically respond.

PERMISSION 3.1: Received frames that do not comply with this control octet(3) content MAY be ignored.

3.3.4. Octet 4 - Source Address

The content of octet 4 must be the source node ID number, from 1 to 31 or 0000 0001b to 0001 1111b.

3.3.5. Information Field

The information field is undefined at this time. The maximum length of the information field must not exceed 512 bytes.

3.3.6. Frame Check Sequence(FCS)

The FCS is a CRC-16 specified by ref. #6.

3.3.7. Closing Flag

Per HDLC (ref. # 6), hex 7E or binary 0111 1110b.

3.4. Message Bus Modules - Basic Description

VME bus modules optionally connect to the message bus in order to provide:

- A secondary control channel for redundancy purposes.
- A diagnostic channel to allow communication between modules if the VME system bus is inoperative.
- A low latency command and status channel to facilitate communications between tightly coupled processes in various system modules.
- Out-of-chassis command channel for multi-chassis systems using SCSA inter-chassis links.

OBSERVATION 3.5: VME commercial CPU boards should provide message bus access in order to fully benefit from the above advantages.

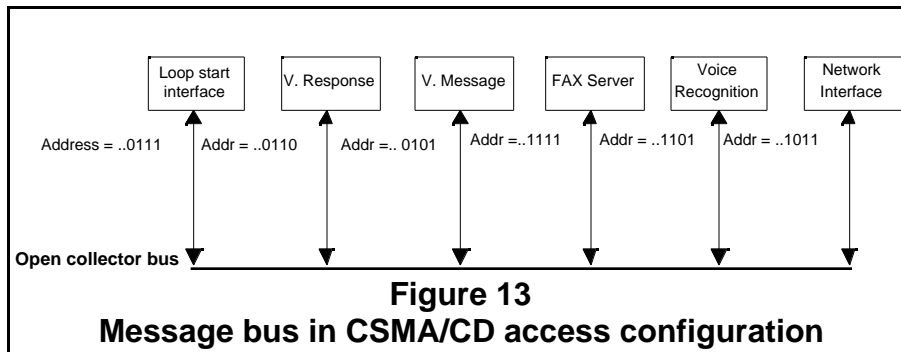
3.5. Typical Message Bus Operation

3.5.1. Message Bus Contention

RULE 3.7: Bus collisions SHALL result in the suspension of transmission by the detecting node. Message bus contention is detected by bitwise comparing transmitted data with the data received from the bus. If a data mismatch is detected (a '1' becomes a '0'), the transmit frame SHALL be immediately aborted, the idle code ('1') SHALL be transmitted and the module SHALL suspend transmission.

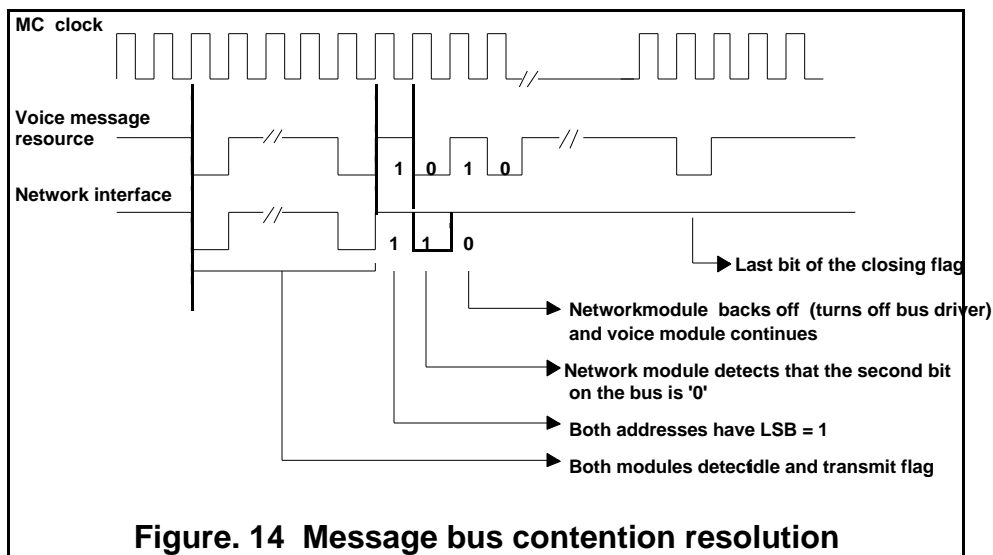
RULE 3.8: Re-transmission SHALL only be initiated after 8 consecutive '1's are received(also see section 3.5.3).

The following diagram illustrates the contention operations:



The system example in Figure 12 consists of six boards. In actuality, each board uses the SCbus slot ID signals, SL0-SL4, as message bus source and destination node addresses. In Figure 12, a voice resource board is assigned an address 0101, and a network board is assigned an address 1011. Assume that two other boards are trying to use the message bus to send messages to these boards and both start to transmit at the same time. The resulting collision is detected by the board sending to the network board when it sends its second destination address bit which is a "1" and detects that the actual value on the bus is a "0" which is the second address bit of the voice board. The board sending to the network board then suspends transmission on the next bit time. If two boards simultaneously attempt to send a message to the same destination node address (fig. 11 octet 2) collision will not occur until the source addresses are sent (octet 4).

Figure 13 illustrates the detail of message bus contention resolution.



3.5.2. Initialization

RULE 3.8: All MC signal drivers SHALL be turned off when the power is initially applied to equipped modules and remain in this state until the message bus controller is initialized.

3.5.3. Equal Access

In order to provide all boards in the system with equal access to the message bus, the following are to be complied with:

RULE 3.9: Message transmission SHALL NOT be allowed while the message bus is not idle.

RULE 3.10: A given message bus agent SHALL NOT be allowed to transmit two back-to-back messages while there may be another message bus agent waiting. Therefore, after a message bus agent has successfully transmitted a message a mandatory 10 bit-time delay SHALL be applied before starting transmission of a second or subsequent message.

RULE 3.11: The message information field size SHALL NOT exceed 512 bytes. This is equivalent to about 2.1 milliseconds in time. All longer messages SHALL be segmented prior to transmission.

3.6. Message Bus - Timing Rules and Observations

The message bus detailed timing relationships is illustrated by the diagram of Figure 14. Refer to Table 7 for a description of the detailed timing values for Figure 14.

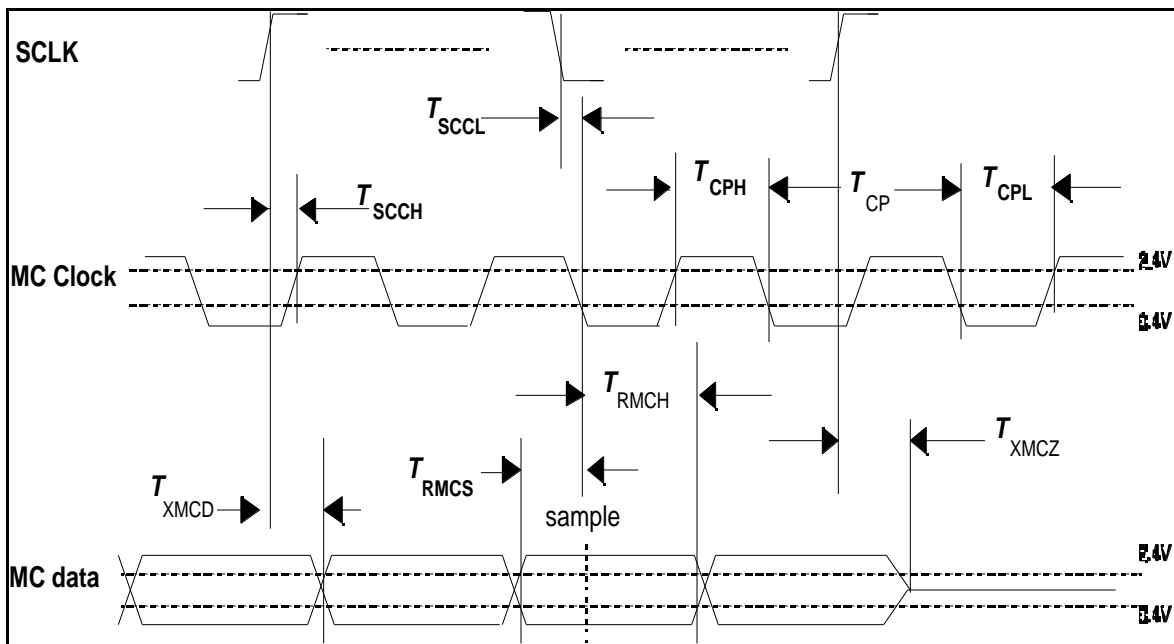


Figure 15 Detailed Message Bus Timing

3.7. Message Bus Electrical Requirements

Symbol	Descriptions	Min	Typical	Max	Unit
Tsccl	SCLK low to MC clock low delay	0		30	
Tscch	SCLK high to MC clock high delay	0		30	
Tcph	Clock period high at 2.048M Hz (SCLK@2) (SCLK@4) (SCLK@8)	237 359 300	244 366 305	252 374 310	ns
Tcpl	Clock period low at 2.048M Hz (SCLK@2) (SCLK@4) (SCLK@8)	237 114 168	244 122 183	252 129 198	ns
Tcp	Clock period at 2.048M Hz	483	488	493	ns
Txmcd	Output data delay -- from SCLK rising edge to valid output or output enabled on the bus. A specification for the transmitter.	0		55	ns
Trmcs	Input data set up time -- from valid data to the falling edge of the MC clock. A specification for the receiver.	25			ns
Trmch	Input data hold time -- from MC clock falling edge until a data change. A specification for the receiver.	30			ns
Txmcz	Output disable delay-- from the SCLK rising edge to output disabled. A specification for the transmitter.	0		35	ns

Table 7 - Message Bus Timing Description

Notes: Txmcz measured with 220/330 Ohm terminator and 20 pF load.

Tcph, Tcpl assume MC clock per recommendation 3.1

3.7.1. Bus Drivers and Receivers

If the SC2000 SCbus interface device is not used(see ref. #5), message bus agent boards should use a TTL-compatible, open-collector type driver with 24 mA or more sinking capability.

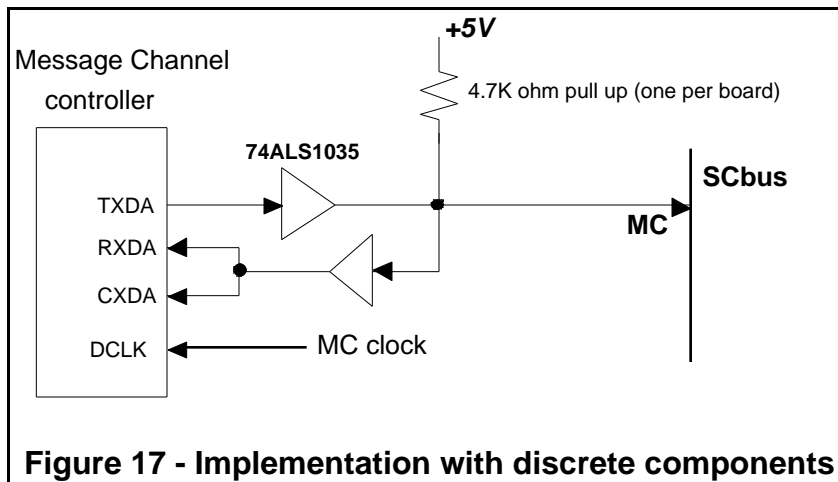
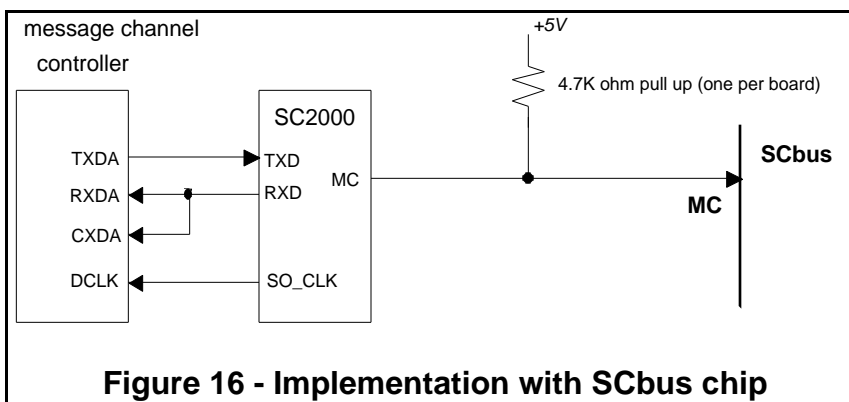
RECOMMENDATION 3.2: The maximum load per board on the bus should not exceed 15 pF capacitance (including the connector).

3.7.2. Bus Terminations

RULE 3.12: Each SCbus module SHALL provide a 4.7 KOhm pull-up to +5 volts on the MC signal line.

RULE 3.13: Each SCbus module SHALL have all on-board message bus driver outputs tied together and pulled up by one 4.7K Ohm resistor. Figure 15 and 16 illustrate typical methods for driving the SC message bus signal MC.

RULE 3.14: Each SCbus module SHALL pull up the MC signal as shown in Figures 15 and 16 even if the message bus is not used.



3.7.3. DC Characteristics

Table 8 contains the dc requirements of the message bus interface devices.

Parameter	Symbol	Min	Max	Unit
Operating voltage	VCC	4.75	5.25	Volt
High level input voltage	V _{iH}	2.00	5.25	Volt
Low level input voltage	V _{iL}	-0.25	0.80	Volt
Input leakage current	I _{LH} or I _{LL}		±10	uA
Output Low current at 0.4V	I _{OL}	24		mA

Table 8 Message Bus Interface Device Characteristics

All input and output requirements are referenced to the SCbus. Most of the advanced CMOS devices with TTL input threshold level, meet the above electrical characteristics.

3.7.4. Loading Limitations

RULE 3.15: A total of 32 drivers maximum SHALL be connected one electrical message bus.

RULE 3.16: A maximum of 21 physical boards, each with one termination resistor, SHALL be connected to one electrical message bus.

OBSERVATION 3.6: The message bus is pulled-up by a resistor on each board. Therefore, no additional backplane terminations should be used.

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CHAPTER 4

4. Board Slot ID

4.1. Introduction

The VME64 system standard(ref. #3) specifies an autoslot ID mechanism that, while workable, is not universally supported. The operation, administration, maintenance and provisioning(OAM&P) objectives of VME-SCSA systems require a positive means to identify SCSA system board locations.

Board slot ID capability is implemented with a set of inputs that provide a means for an equipped VME-SCSA compatible board to determine it's physical slot or geographic address in the card cage it occupies. This is needed for several reasons.

-This ID provides a board address for SCSA compatible VME boards that have implemented message bus.

-It allows slot-associated I/O or telephony trunks to be logically associated with particular system boards for diagnostic and maintenance purposes.

-It provides a positive means of identification for system boards that do not have a VME system bus. This is usually necessary for downloader and interrupt use.

4.2. Slot ID Signals

The five slot ID signals SL0*-SL4* are inverted polarity logic level signals that receive a five bit, binary-encoded geographic address from the VME backplane with ID's ranging from 1 to 21.

RULE 4.1: SCSA compliant J2/P2 backplanes SHALL uniquely binary encode each intended SCSA physical board location, starting from the leftmost slot viewed from the card insertion side of the card cage as slot number "1".

RULE 4.2: The backplanes SHALL encode intended SCSA slots by strapping the appropriate SL0*-SL4* signals to dc ground with a resistance not to exceed 100 Ohms. SL0* SHALL be the least significant binary bit and SL4* the most significant.

RULE 4.3: SCSA Compliant backplanes SHALL NOT use a slot ID code of zero or 00000b(SL0*-SL4* open) .

RULE 4.4: The system software SHALL reserve binary code 00000b, obtained when NO slot ID signals are strapped to ground, for non-compliant backplanes that do not provide slot ID signals.

RULE 4.5: Each SCSA compatible VME board implementing slot ID SHALL apply +5 Volts through a resistor of 10 KOhms to 100 KOhms to each of the slot ID signal nets.

PERMISSION 4.1: Backplanes may delete slot ID's from one or more of the card slots for use by non-SCSA compliant boards such as a CPU or bus controller which normally do not use an SCSA slot ID.

RULE 4.6: Even if slot ID's are not contiguous, the encoded backplane slot ID's SHALL correspond to the physical slot positions counting from the leftmost slot looking at the card insertion opening of the cage.

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CHAPTER 5

5. SCbus Electrical Specifications

5.1. Introduction

SCbus is a bit-serial, byte oriented, synchronous, TDM bus. Voice/data transfer on the bus is accomplished by assigning one or more time-slot IDs and a bus stream number(SDn plus time-slot number) to the sender and receiver. At the selected time-slot, the software selected sender drives the bus and somewhere in the system a receiver clocks-in the data bits. There is no handshake or confirmation taking place between the sender and the receiver(s). The operation is solely based on the assumption that all boards in the system are under software control, use the SCLK for bit registration and have their time-slot counters reset by using the FSYNC* frame sync pulse.

5.2. Electrical Signal Characteristics

All input and output signal requirements are with reference to the SCbus grounds. Most advanced CMOS devices with TTL input threshold level meet the electrical characteristics specified in Table 9.

Parameter	Symbol	Min	Max	Unit
Operating voltage	VCC	4.75	5.25	Volt
High level voltage range	V _{iH}	2.00	5.25	Volt
Low level voltage range	V _{iL}	-0.25	0.80	Volt
Input leakage current	I _{LH} or I _{LL}		±10	uA
Output High current at 2.4V	I _{OH}	-24		mA
Output Low current at 0.4V	I _{OL}	24		mA
Output off-state leakage current	I _{LZ}		10	uA

Table 9 - SCbus interface device DC conditions

5.3. Bus Driving and Receiving Requirements

RULE 5.1: All SCbus transport bus(SDn) drivers SHALL be TTL-compatible tri-state type drivers with 24 mA. minimum drive capability.

It is recommended that receivers with input hysteresis (or Schmitt-trigger) be used on all clock inputs.

The maximum load on any SCbus signal imposed by one system module should not exceed +/-150 uA and 15 pF capacitance (including the connector).

5.4. Signal Line Interconnections

A controlled impedance backplane should be used if the 8.192 MHz SCbus clock rate is desired. It is intended that the SCbus backplane be similar in construction and electrical characteristics to that used for the VME system bus. A fully loaded SCbus backplane effective impedance of at least 50 Ohms is required to preserve fanout and signal quality.

RECOMMENDATION 5.1: The backplane impedance characteristics should adhere to those specified in reference #2 or #3, section 6.5.2.

PERMISSION 5.1: If a 24 mA capable interface device is used, up to 32 of these devices may be connected to the SC data bus.

PERMISSION 5.2: Ribbon cable may be used to interconnect SCbus modules if the SCLK bus clock is reduced to 4.096 M bps and the 21 slot restriction is observed. External terminations should not be used with ribbon cabled SCbus(see section 5.5).

OBSERVATION 5.1: The use of a ribbon cable for the SCbus module interconnect with a generic J2/P2 backplane requires manual wiring of the SL0* to SL4* slot selection signals(see chapter 4) for systems requiring geographic addresses.

5.5. Signal Line Terminations

5.5.1. Serial Voice/Data(SD) Bus

RULE 5.2: Each SCbus module SHALL provide a 33 KOhm pull-up to +5 volts on each SD signal line.

RULE 5.3: For SCbus operation at 8M bps each SD bus line SHALL be terminated by a 470/680 Ohm pull-up/pulldown network at the electrical ends of the backplane.

PERMISSION 5.3: If an SCbus PCB backplane is used that is less than or equal to 4.8 inches long(seven VME slots) a single 220/330 Ohm pull-up/pull-down terminator network may be used on each SD line, installed at the center of the backplane section.

5.5.2. Clocks and FSYNC*

RULE 5.4: Each SCbus module, either clock master or slave, SHALL provide a 33 KOhm pull up to +5 Volts for the SCLK, SCLK*2, FSYNC* and SREF8K signal lines.

RULE 5.5: For SCbus operation at 8M bps the clocks and FSYNC* should be terminated by a 470/680 Ohm pull-up/pulldown network at the electrical ends of the backplane.

If the PC backplane is 4.8 inches or shorter PERMISSION 5.3 also applies to these signal lines.

5.5.3. CLKFAIL

RULE 5.6: The SCbus CLKFAIL signal SHALL be pulled-up to +5 Volts by one 4.7K pull up resistor on each clock master module.

CHAPTER 6

6. Mechanical Specifications

6.1. Introduction

The SCbuses are defined to use the VME 6U format J2/P2 connector. The basic mechanical parameters are contained in references #2 and #3. The SCbuses also coexist with the existing VME64 system bus extensions while also retaining 32 user defined pins for I/O connectivity.

6.2. VME Bus Backplane Connectors and VME Board Connectors

6.2.1. SCbus Connector

The VME-SCbus uses 32 pin locations of rows (a) and (c) of the VME J2/P2 connector as defined in IEEE 1014-1987, section 7.6. The maximum length of a PCB backplane that will operate reliably at all defined SCSA bus speeds has been determined to be 21 slots.

6.2.2. VME board PCB layout

To ensure the reliability and consistent performance of the SCbus, individual SCbus signals brought into a circuit board should not have trace lengths longer than 3 inches. If a bus signal is to be terminated at more than one place, each trace should start at the P2 connector and the aggregate stub lengths should be less than 4.5 inches.

6.2.3. J2/P2 SCbus Backplane

SCbus provides the highest signal to noise ratio and minimized crosstalk and reflections when implemented across a controlled impedance, multi-layer printed circuit backplane. This is mandatory in order to run at the highest defined SCbus speed of 8.192 M bps. Care should be exercised in the backplane layout to ensure minimum crosstalk from the VME 32 bit system bus signals on row(b) of J2/P2 to the SCbus signals. An enhanced, 5 row DIN connector further improves SCbus signal quality.

RECOMMENDATION 6.1: A ground plane should be placed between the SCbus signals and the VME64 J2/P2 system bus (row b) extension signals.

The pinout of the J2/P2 connector(see Table 10) was selected to permit a connector adapter from the J2/P2 connector to a 26 conductor ribbon cable. Ribbon may be used for SCbus module "island" interconnection or for mixed VME-ISA system use if the maximum length of 21 slots is not exceeded. Care should also be exercised in the power layout of mixed systems in order to avoid ground potential differences that will reduce dc operating and transient voltage margins.

RULE 6.1: Reserved pin 14(a) on table 10 SHALL NOT be connected to circuitry on any compliant board.

RULE 6.2: Reserved pin 14(a) on table 10 SHALL be bused on compliant backplanes.

6.2.4. VME SCbus J2/P2 PIN ASSIGNMENT

Pin #	Row (a)	Row (b)	Row (c)
1	SD_15	+5V	MC
2	SD_13	GND	SD_14
3	GND	RETRY	SD_12
4	SD_10	A24	SD_11
5	SD_8	A25	SD_9
6	GND	A26	SD_7
7	SD_5	A27	SD_6
8	SD_3	A28	SD_4
9	SD_1	A29	SD_2
10	SD_0	A30	GND
11	Fsync*	A31	CLKFAIL
12	SCLK	GND	SREF8k
13	SCLKx2*	+5 V	GND
14	Reserved(bus	D16	SL_4*
15	SL_3*	D17	SL_2*
16	SL_1*	D18	SL_0*
17	User I/O	D19	User I/O
18	User I/O	D20	User I/O
19	User I/O	D21	User I/O
20	User I/O	D22	User I/O
21	User I/O	D23	User I/O
22	User I/O	GND	User I/O
23	User I/O	D24	User I/O
24	User I/O	D25	User I/O
25	User I/O	D26	User I/O
26	User I/O	D27	User I/O
27	User I/O	D28	User I/O
28	User I/O	D29	User I/O
29	User I/O	D30	User I/O
30	User I/O	D31	User I/O
31	User I/O	GND	User I/O
32	User I/O	+5 V	User I/O

Table 10 - J2/P2 Pin Assignments

Note: Row (b) contains VME system bus extensions and is taken from ref. #2, section 7.6.2, Table 54: J2/P2 pin assignments.

CHAPTER 7

7. Inter-chassis Link Facilities(this chapter is informative only)

7.1. Introduction

The intent of this section is to establish broad guidelines for the development of inter-system links for the purpose of resource sharing, call routing, and overall redundancy as though provided by one large system.

Link cards are needed to exchange some or all of the SCbus timeslots within one VME chassis to another electrical SCbus system. The mapping of the SCbus backplane timeslots through the link card will require a low level software driver that would need to be integrated into the SCSA switching and routing model to permit full flexibility inter-system sharing. The identity of timeslots should be preserved though the link.

There are many proprietary and public domain communication link media that could serve the needs of SCSA systems. It is hoped that exposing this need along with a set of general guidelines will promote the development or adaptation of appropriate link boards into the VME-SCSA system environment.

The network topologies of interconnected call processing systems likewise remains open for innovation. The expected variation in classes of call processing systems will likely permit a number of inter-chassis link products that are more or less optimized for a given system node count or other special requirements, i.e.: non-blocking access, low through-delay, etc.

Potential inter-chassis link topologies and overall call processing system attributes follow:

-Point to point: This link type can provide low cost inter-chassis connectivity. The media can even be optical. Although, if more than two systems are to be interconnected these costs rise quickly due to the link-board-per-node requirement. System resilience is good.

-Logical bus: A bus can also provide a low cost implementation for systems where relatively small amounts of information are to be exchanged between nodes. System resilience is also good.

-Ring topology: provides good connectivity at moderate cost. Traditional token based access schemes are somewhat difficult to administrate. Rings may have limited bandwidth and also have undesirable link failure modes unless more costly redundant rings are employed.

-Star topology provides the largest system expansion capability with the possibility to provide a hub that scales with the overall system requirements up to a complete non-blocking, single layer switch emulation. The hub itself is, however, a single point of failure that can disable an entire system.

7.2. SD bus link Requirements:

Link boards that transport data bus timeslot content between SCbuses in physically independent SCSA systems need to generally adhere to just a few guidelines. These are:

-Preserve frame structure. This means that the exact relationship between all timeslots in a given frame of 16 SD signal should be reconstructed faithfully at the remote end. This is necessary not only to ensure reliable transport but also to permit the use of hyperchannel data paths for the purpose of transporting wideband signal and data streams.

-Permit remote synchronization. The remote system may not have access to network synchronization. It would then be necessary for the remote SCbus system to obtain frequency locked clocking through the link and to become an SCbus clock master or drive signal SREF8K in the remote system.

-Limit delay. Most large system implementations need to limit delay through the entire system connection to 1 or 2 milliseconds end to end, at most, for echo cancellation purposes. If local echo cancellation is performed at each 4-wire digital to 2-wire analog conversion point in the system and no conferencing is done across nodes, this delay limit can be extended to 18 ms. This delay limit would permit ATM packet based system interconnects.

-Synchronous switching. Any changes in signal path should be performed during times when affected timeslots are inactive.

-Switchpath coherency. A positive means to establish a "virtual" circuit(VC) path to all intended nodes needs to be included. A VC "token" assigned by the system software can be passed to each interchassis link card of intended connection using the message bus or other link. Local association of the VC token to the physical interchassis transport media map may then be assigned and then sent to the other nodes for extraction of data from the link. The VC token method provides traceability to the source node.

7.3. Message Bus

The message bus is edge-synchronized to the SCbus clocks for the purpose of contention resolution. This makes the layer 1(physical) interconnection of the local message bus with a remote chassis message bus difficult. Therefore, an intelligent link board would preferably implement a low delay gateway or routing function depending on the system topology and media used.

The message bus upper layer protocols are still in definition at this time but are not dependent on data link parameters. The overall message channel inter-chassis requirements are:

-Message receipt and address decoding. A software-provided routing map would need to be downloaded into the link board to determine whether the message is intended for an in-chassis or out of chassis destination. If an out of chassis address is determined, the message would be queued for transmission to other system nodes. The local message channel packet acknowledgment would then also need to be fulfilled.

-Reliable transport. A buffered four layer transport facility to all remote chassis' should be provided to ensure reliable delivery and routing of messages.

-High speed transport. In many instances, real time switching and other commands may be sent over the message channel. An SCbus-to SCbus delay of under ten milliseconds is a suggested design limit.

-Interface with local message bus. Received messages should be retransmitted on the local message bus including possible bus access retries and possible initiation of invalid destination reply messages to the originating node.

Appendix A
(Normative and Informative)

Bibliography

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